MP1701B
Pulse Pattern Generator
Operation Manual

Third Edition

Read this manual before using the equipment.
Keep this manual with the equipment.

ANRITSU CORPORATION

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Safety Symbols

To prevent the risk of personal injury or loss related to equipment malfunction, Anritsu Corporation uses the following safety symbols to indicate safety-related information. Insure that you clearly understand the meanings of the symbols BEFORE using the equipment.

Symbols used in manual

DANGER	This indicates a very dangerous procedure that could result in serious injury or death if not performed properly.
WARNING	This indicates a hazardous procedure that could result in serious injury or death if not performed properly.
CAUTION	This indicates a hazardous procedure or danger that could result in light-to-severe injury, or loss related to equipment malfunction, if proper precautions are not taken.

Safety Symbols Used on Equipment and in Manual

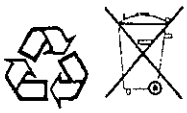
(Some or all of the following five symbols may not be used on all Anritsu equipment. In addition, there may be other labels attached to products which are not shown in the diagrams in this manual.) The following safety symbols are used inside or on the equipment near operation locations to provide information about safety items and operation precautions. Insure that you clearly understand the meanings of the symbols and take the necessary precautions BEFORE using the equipment.

This indicates a prohibited operation. The prohibited operation is indicated symbolically in or near the barred circle.

This indicates an obligatory safety precaution. The obligatory operation is indicated symbolically in or near the circle.

This indicates warning or caution. The contents are indicated symbolically in or near the triangle.

This indicates a note. The contents are described in the box.



These indicate that the marked part should be recycled.

MP1701B Pulse Pattern Generator
Operation Manual

May 1992 (First Edition)
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Printed in japan

For Safety

Repair

WARNING ⚠

Falling Over

WARNING

1. Always refer to the operation manual when working near locations at which the alert mark shown on the left is attached. If the operation, etc., is performed without heeding the advice in the operation manual, there is a risk of personal injury. In addition, the equipment performance may be reduced.
   Moreover, this alert mark is sometimes used with other marks and descriptions indicating other dangers.
2. When supplying power to this equipment, connect the accessory 3-pin power cord to a 3-pin grounded power outlet. If a grounded 3-pin outlet is not available, before supplying power to the equipment, use a conversion adapter and ground the green wire, or connect the frame ground on the rear panel of the equipment to ground. If power is supplied without grounding the equipment, there is a risk of receiving a severe or fatal electric shock.
3. This equipment cannot be repaired by the user. DO NOT attempt to open the cabinet or to disassemble internal parts. Only Anritsu-trained service personnel or staff from your sales representative with a knowledge of electrical fire and shock hazards should service this equipment. There are high-voltage parts in this equipment presenting a risk of severe injury or fatal electric shock to untrained personnel. In addition, there is a risk of damage to precision parts.
4. This equipment should be used in the correct position. If the cabinet is turned on its side, etc., it will be unstable and may be damaged if it falls over as a result of receiving a slight mechanical shock.

For Safety

CAUTION

Changing Fuse

CAUTION ⚠

1. Before changing the fuses, ALWAYS remove the power cord from the poweroutlet and replace the blown fuses. Always use new fuses of the type and rating specified on the fuse marking on the rear panel of the cabinet.

   T☐☐☐ A indicates a time-lag fuse.
   ☐☐☐A or F ☐☐☐ A indicate a normal fusing type fuse.

   There is risk of receiving a fatal electric shock if the fuses are replaced with the power cord connected.

Cleaning

2. Keep the power supply and cooling fan free of dust.
   - Clean the power inlet regularly. If dust accumulates around the power pins, there is a risk of fire.
   - Keep the cooling fan clean so that the ventilation holes are not obstructed. If the ventilation is obstructed, the cabinet may overheat and catch fire.

3. Use two or more people to lift and move this equipment, or use a trolley. There is a risk of back injury, if this equipment is lifted by one person.

Equipment Certificate

Anritsu Corporation certifies that this equipment was tested before shipment using calibrated measuring instruments with direct traceability to public testing organizations recognized by national research laboratories including the Electrotechnical Laboratory, the National Research Laboratory and the Communication Research laboratory, and was found to meet the published specifications.

Anritsu Warranty

Anritsu Corporation will repair this equipment free-of-charge if a malfunction occurs within 1 year after shipment due to a manufacturing fault, provided that this warranty is rendered void under any or all of the following conditions.

- The fault is outside the scope of the warranty conditions described in the operation manual.
- The fault is due to misoperation, misuse, or unauthorized modification or repair of the equipment by the customer.
- The fault is due to severe usage clearly exceeding normal usage.
- The fault is due to improper or insufficient maintenance by the customer.
- The fault is due to natural disaster including fire, flooding and earthquake, etc.
- The fault is due to use of non-specified peripheral equipment, peripheral parts, consumables, etc.
- The fault is due to use of a non-specified power supply or in a non-specified installation location.

In addition, this warranty is valid only for the original equipment purchaser. It is not transferable if the equipment is resold.

Anritsu Corporation will not accept liability for equipment faults due to unforeseen and unusual circumstances, nor for faults due to mishandling by the customer.

Anritsu Corporation Contact

If this equipment develops a fault, contact the head office of Anritsu Corporation at the address in the operation manual, or your nearest sales or service office listed on the following pages.

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POWER SUPPLY VOLTAGE

Line Voltage Selection

This instrument is operable on a nominal voltage of 100 to 127 Vac (AC 100 V system) or 200 to 250 Vac (AC 200 V system) by setting the AC 100 V/AC 200 V switch under the left side cover.

The voltage and current ratings are indicated on the rear panel when the instrument is shipped from the factory.

To operate on the other voltage system, change the AC 100 V/AC 200 V switch setting. The plate on the rear panel indicating the voltage and current ratings should be changed to the appropriate one. Order the plate from Anritsu Corporation if needed.

In this manual, the power supply voltage and current ratings are represented by **Vac and ***A, respectively.

Relationship Between Voltage, Current and Fuse

The relationship between power supply voltage and current ratings is shown below:

**Vac	***A
100 to 127 Vac (AC 100 V system)	8A (T8A Fuse)
200 to 250 Vac (AC 200 V system)	6.3A (T6.3A Fuse)

STORAGE MEDIUM

This equipment stores data and programs using floppy disk.

Data and programs may be lost due to improper use or failure.

ANRITSU therefore recommends that you back-up the memory.

ANRITSU CANNOT COMPENSATE FOR ANY MEMORY LOSS.

Please pay careful attention to the following points. Do not remove the floppy disk from equipment being accessed.

For details refer to the relevant operation manual.

(Floppy disk)

- Observe the specified environmental conditions. Also, do not use the equipment in a dusty place.
- Keep magnetic objects away from the disk. Do not bend the disk.
- Insert the head protection sheet into the disk slot when moving the equipment.

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Power Line Fuse Protection

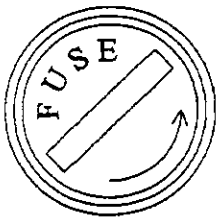
For safety, Anritsu products have either one or two fuses in the AC power lines as requested by the customer when ordering.

Single fuse: A fuse is inserted in one of the AC power lines.

Double fuse: A fuse is inserted in each of the AC power lines.

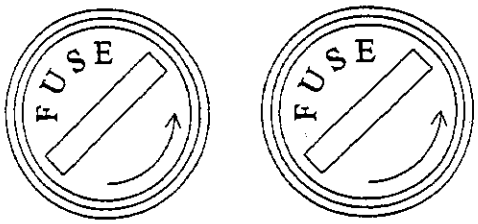
Example 1: An example of the single fuse is shown below:

Fuse Holder



Example 2: An example of the double fuse is shown below:

Fuse Holders



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SECTION 1
GENERAL

1.1 General

The MP1701B Pulse Pattern Generator operates at clock frequencies from 50 MHz to 10 GHz and generates two patterns: pseudorandom pattern (PRBS) and programmable pattern. The PRBS pattern can have one of 7 periods ranging from 2^7-1 to 2^{31}-1. The programmable pattern has data and word modes, and can generate patterns that have a maximum length of 512k bits. For the output interface, the offset can be set in 5 mV steps, the amplitude can be set in 10 mV steps and the delay between output data signal and clock signal can be set in 1 ps steps.

The clock signal can be supplied from the outside or from an internal clock generator. The internal clock generator frequency can be set from 50 MHz to 10 GHz in 1 kHz steps.

1.2 Manual Composition

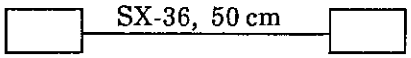
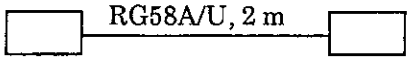
Two manuals are related to handling of the MP1701B Pulse Pattern Generator: this manual and the GP-IB operation manual. When controlling the MP1701B remotely via a GP-IB, refer to the GP-IB operation manual. The GP-IB operation manual is common to the MP1701B, MP1608A, and MP1650A Pulse Pattern Generators.

1.3 Composition

1.3.1 Standard composition

The standard composition of the MP1701B Pulse Pattern Generator is shown in Table 1-1.

Table 1-1 Standard Composition

Item	No.	Name	Qty	Remarks
Instrument	1	MP1701B Pulse Pattern Generator	1	
Accessories supplied	2	Fuses	2	MF51NR8A (8A, F0071) or T6.3A 250 V (6.3A, F0014)
	3	Semirigid cable	2	SMA-P *1 SMA-P  J0500A
	4	Coaxial cable	2	BNC-P BNC-P  J0127B
	5	Adapter	6	APC3.5-J-J Connector, J0496
	6	3.5-inch floppy disk	2	2HD *2, Z0054
	7	GP-IB cable	1	2 m, J0008, 408JE-102
	8	Power cord	1	2.6 m, shielded, 13 A, J0491
	9	Operation manual	1	W0512AE
	10	GP-IB operation manual	1	W0520AE

*1 UT-141AA equivalent semirigid cable

*2 3.5-inch floppy disks are formatted.
Stores the PRBS 2^{10}-1 equivalent (mark ratio 1/2, 1/4, 1/8) patterns that can be generated by the Anritsu MP1601A and MP1604A Pulse Pattern Generators in one disk.
Another disk is empty.

1.4 Optional Accessories and Peripheral Devices

The MP1701B optional accessories and peripheral devices (sold separately) are shown in Table 1-2.

Table 1-2

Model No./ Order No.	Name	Remarks
J0500A	Semirigid cable, 0.5 m	SMA-P·SX-36·SMA-P
J0500B	Semirigid cable, 1 m	SMA-P·SX-36·SMA-P
J0322A	Coaxial cable, 0.5 m	SUCOFLEX 104, 11SMA-11SMA
J0322B	Coaxial cable , 1 m	SUCOFLEX 104, 11SMA-11SMA
J0498	Coaxial cable, 0.5 m	APC 3.5-P· —— · APC 3.5-P*
J0499	Coaxial cable, 1 m	APC 3.5-P· —— · APC 3.5-P*
		*Double shielded coaxial cable used
J0007	GP-IB cable , 1 m	408 JE-101
J0008	GP-IB cable, 2 m	408 JE-102
J0127B	Coaxial cable, 2 m	BNC-P·RG58A/U·BNC-P
J0496	APC 3.5J-J connector	
Z0054	3.5 inch floppy disk	2HD
MB24B	Portable Test Rack	
B0171	Carrying case	
B0163	Transport bag	
B0044	Rack mount kit	IMW-5U
PACKET V	Personal Technical Computer	Used as system controller

1.5 Specifications

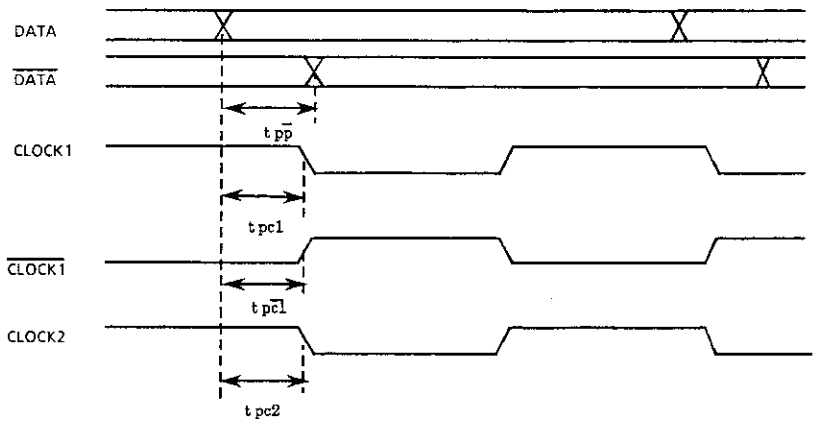
Operation frequency range	Internal clock		0.05 to 10 GHz		
	External clock		0.05 to 10 GHz		
External clock	Input level		0.7 to 2.0 Vp-p		
	Waveform		0.05 to 0.5 GHz: square wave (duty factor: 50%) >0.5 GHz: sinusoidal or square wave (duty factor: 50%)		
	Connector		APC 3.5 (with female to female adaptor)		
Internal clock	Frequency range		0.05 to 10 GHz		
	Resolution		1 kHz, 1 MHz		
	Frequency accuracy		± 1 ppm		
	SSB phase noise		At 10 kHz offset ≦ -85 dBc/Hz (0.05 to <4.0 GHz) ≦ -80 dBc/Hz (4.0 to <8.0 GHz) ≦ -75 dBc/Hz (8.0 to 10 GHz)		
	Reference signal		10 MHz (INT/EXT selectable)		
Pattern generation	Pseudorandom binary sequence pattern (PRBS)	Pattern length	2^N-1: N = 7, 9, 11, 15, 20, 23, 31		
		Mark ratio	1/2, 1/4, 1/8, 0/8 (1/2, 3/4, 7/8, 8/8 also possible by logic inversion)		
		Number of "AND bit" shifts when setting mark ratio	1 bit or 3 bit (Selectable using rear panel DIP switch)		
	DATA pattern	Data length	2 to 524288 bits	Data length	Step width
				2 to 4096	1 step 524288/128 = 4096
				4224 to 524288	128 step 128N (N = 33 to 4096)
		Pattern reset/preset	ALL/PAGE selectable		

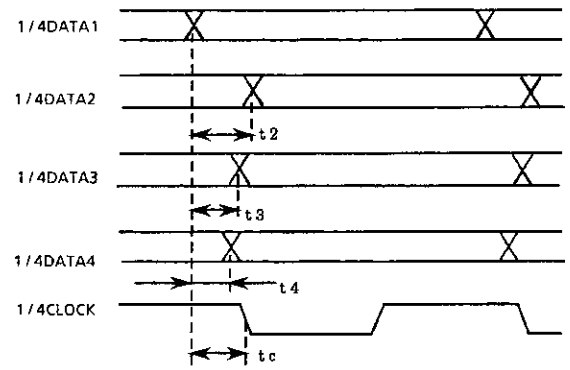
Pattern generation (Cont.)	Word pattern	Word length	2 to 16 bits
		Number of words	1 to 32768
		Pattern reset/preset	ALL/PAGE selectable

Relationship between Word Length and Number of Words

Word length N	Number of Words			
	Range	Step width	Range	Step width
2	1 to 2048	1 step	2112 to 32768	64 step
3	1 to 1365	1 step	1408 to 32768	128 step
4	1 to 1024	1 step	1056 to 32768	32 step
5	1 to 819	1 step	896 to 32768	128 step
6	1 to 682	1 step	704 to 32768	64 step
7	1 to 585	1 step	640 to 32768	128 step
8	1 to 512	1 step	528 to 32768	16 step
9	1 to 455	1 step	512 to 32768	128 step
10	1 to 409	1 step	448 to 32768	64 step
11	1 to 372	1 step	384 to 32768	128 step
12	1 to 341	1 step	352 to 32768	32 step
13	1 to 315	1 step	384 to 32768	128 step
14	1 to 292	1 step	320 to 32768	64 step
15	1 to 273	1 step	384 to 32768	128 step
16	1 to 256	1 step	264 to 32768	8 step

Pattern generation (Cont.)	External pattern input mode	Number of channels	8 CH (1 to 8 CH input settings are possible)
		Pattern bit rate	1/8 speed of fundamental clock
		Clock output *1	ECL, 50 Ω, connected with −2 V *1 Output of clock for external 1/8 pattern generation
		External pattern input level	ECL, 50 Ω, connected with −2 V
		Connector	SMA
	Logic inversion		possible
	Error insertion	Error rate	10^{-n}: n = 4, 5, 6, 7, 8, 9 and single
		Insertion position	possible to insert into any 1 CH of 32 CH (Selectable with rear panel switch)
DATA output	Waveform format		NRZ
	Number of outputs		2 (DATA/$\overline{\text{DATA}}$)
	(DATA/$\overline{\text{DATA}}$) tracking mode		ON/OFF selectable
	Amplitude		0.5 to 2 Vp-p, variable in 10 mV steps [Setting error: ≦ ±15%, ±100 mV whichever is greater]
	Offset voltage		Voltage: −2 to +2 V (V_{OH}), variable in 5 mV steps [Setting error: ≦ ±15%, ±100 mV or ±15% of amplitude whichever is greatest] Display mode: V_{OH}, V_{TH}, V_{OL}, selectable
	Rise/fall time		≦ 30 ps
	Pattern jitter		≦ 25 ps
	Crosspoint adjust function		DATA, $\overline{\text{DATA}}$, adjustable, independently
	Waveform distortion		<10% or <100 mV, whichever is greater
	Load impedance		50 Ω (with back termination)
	Connector		APC 3.5 (with female to female adaptor)

CLOCK output	Number of outputs	3 (CLOCK 1, $\overline{\text{CLOCK 1}}$, CLOCK 2)
	CLOCK 1, $\overline{\text{CLOCK 1}}$ delay	±500 ps, variable in 1 ps steps
	CLOCK 1, $\overline{\text{CLOCK 1}}$ amplitude	0.5 to 2 Vp-p, variable in 10 mV steps [Setting error: ≦ ±15% or ±100 mV whichever is greater]
	CLOCK 2 amplitude/offset voltage	2 Vp-p (≦ ±15%) fixed/0 V (≦ ±300 mV) fixed
	Offset voltage	Voltage: −2 to +2 V (V_{OH}), variable in 5 mV steps [Setting error: ≦ ±15%, ±100 mV or ±15% of amplitude whichever is greatest] Display mode: V_{OH}, V_{TH}, V_{OL}, selectable
	Rise/fall time	Of 20% to 80% amplitude: ≦30 ps (≧5 GHz) ≦50 ps (<5 GHz)
	Waveform distortion	<10% or 100 mV whichever is greater
	Duty ratio adjust function	Of CLOCK 1, $\overline{\text{CLOCK 1}}$ and CLOCK 2, adjustable independently
	Load impedande	50 Ω (with back termination)
	Connector	APC 3.5 (with female to female adaptor)
Output phase	 $\lvert t_{p\bar{p}} \rvert \leq 30$ ps $\lvert t_{pc1} \rvert \leq 30$ ps $\lvert t_{p\bar{c}1} \rvert \leq 30$ ps $\lvert t_{pc2} \rvert \leq 30$ ps Where CLOCK1/$\overline{\text{CLOCK1}}$ delay is set to 0ps.	

1/4 DATA/ CLOCK output	Number of outputs	DATA: 4 CLOCK: 1
	Output level	0.5 to 1 Vp-p, variable in 10 mV steps [Setting error : ≤ ±15% or ±100 mV whichever is greater]
	Offset voltage	Voltage: −1.5 to +1.5 V (V_{OH}), variable in 5 mV steps [Setting error : ≤ ±150 mV] Display mode : V_{OH}, V_{TH}, V_{OL}, selectable
	Rise/fall time	Of 20% to 80% amplitude ≤ 200 ps
	DATA output jitter	≤ 100 ps
	Waveform distortion	≤ 15%
	Skew	 |t2| ≤ 100ps |t3| ≤ 100ps |t4| ≤ 100ps |tc| ≤ 100ps
	Connector	SMA

Sync signal output	Number of outputs	Pattern : 1 (BNC connector) 1/2 CLOCK: 1 (SMA connector) 1/32 CLOCK: 1 (BNC connector)
	Output level	1 Vp-p ± 20% (V_{OH}: 0 V, ≤ ± 200 mV)/50 Ω
External control		GP-IB (IEEE 488.2)
Ambient temperature, rated range of use		0° to 50°C (However, 5° to45°C applied for pattern memory floppy disk)
Parameter memory	Media	3.5 inch floppy disk (2HD) 1.6 Mbyte (unformat)
	Format	MS-DOS, Rev. 3.1
	Content	Programmable pattern and other parameters
Power		**Vac ± 10% (max. 250 Vac), 48 ~ 63 Hz, ≤ 700 VA
Dimensions and weight		221H x 426W x 450D mm, <33 kg

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SECTION 2
PREPARATIONS

2.1 Installation Conditions

Operating temperature and humidity range	0°C to 50°C (However, 5°C to 40°C for floppy disks), Relative humidity ≦ 95%
Storage temperature and humidity range	-40 to 70°C, Relative humidity ≦ 95%

Use and store the MP1701B within these ranges.

Do not use or store the instrument in locations

- where vibrations are severe.
- where it is damp or dusty.
- where there is exposure to direct sunlight.
- where there is exposure to active gases.

Long-term storage at high temperature will increase the discharge rate of the internal battery. Store the instrument below room temperature.

2.2 Safety Measures

- Use the power cord (an accessory) to connect the instrument to the ac power supply.

  Ground either the ground terminal of the power cord or the frame ground terminal on the rear panel.

- Turn off the POWER switch and disconnect the power cord from the socket before changing the fuse.

  Use a fuse of the same rating.

- If the MP1701B is operated at room temperature after being used, or stored, for a long time at low temperature, condensation may occur and cause short-circuiting. To prevent this, do not turn the power on until the instrument is completely dry.

2.3 Power Supply Voltage

The power supply voltage rating for the MP1701B is shown on the rear panel. Always use a voltage within the rated voltage range. Excessive voltage may damage the circuits.

2.4 Internal Battery Life

The MP1701B uses lithium primary cells as the timer and memory back-up power supply. The life of the cells depends on the temperatures at which the instrument is stored. It is more than 10 years for storage at room temperature.

Storage at high temperature for long periods will shorten this period.

Replace discharge cells: they cannot be recharged.

Since battery replacement can only be made by Anritsu, contact the nearest Anritsu representative when replacement is required.

2.5 Damage Prevention Measures

- When applying signals to the MP1701B, never apply an excessive voltage because the circuits may be damaged.
- The output is terminated at 50 Ω. Do not feed current. The load must be a real resistance of 50 Ω, and should be terminated at ground potential.
- Always ground the equipment to be connected (including the device under test) before connecting the input and output terminals.
- Since the outer shield and center conductors of a coaxial cable act as a capacitor, discharge the shield and center conductors by shorting them with a piece of metal.

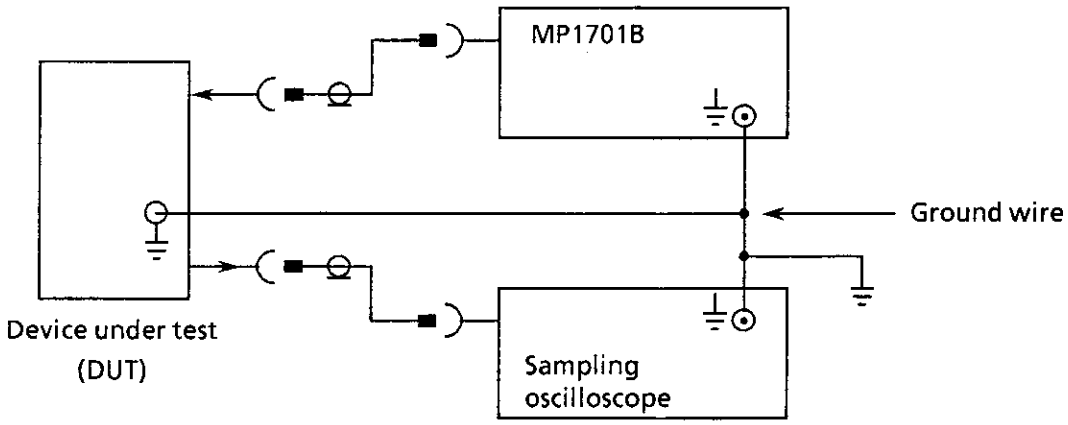

Fig. 2-1 Grounding and Cable Discharging

- The bottom section of the MP1701B includes hybrid ICs and important circuits and parts which are susceptible to static electricity. Do not open it.
- The hybrid ICs used in the MP1701B are air-tight. Do not open them. If they are opened and then do not perform satisfactorily, maintenance service may be refused.
- Ventilation holes exist at the bottom cover. Do not disturb the air flow through the holes.

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SECTION 3
FRONT AND REAR PANELS

3.1 Panel Controls (Figs. 3-1, 3-2 and Table 3-1)

Table 3-1 Panel Control Explanation

No.	Label	Function
①	POWER	Power switch and lamp.
②	GP-IB	GP-IB local key and remote lamp
	REMOTE	Lamp that shows that the MP1701B is in the remote state.
	LOCAL	Key for manual switching from the GP-IB remote state to the local state.
③	PANEL LOCK	Panel lock key and lamp In the panel lock state, all switches and keys other than the POWER switch and panel lock key are disabled.
④	CLOCK	Internal/external clock switch and external clock input connector
	INT/EXT	Internal/external clock switch
	EXT INPUT	External clock input connector
⑤	SYNC OUTPUT	Sync signal output connectors when waveform observed with an oscilloscope.
	1/32 CLOCK	Connector for 1/32 divided output of clock frequency
	PATTERN	Pattern sync output connector

Table 3-1 Panel Control Explanation (Cont.)

No.	Label	Function
⑥	PRESET	Programmable pattern preset function
	ALL 0	Sets all bits to 0.
	ALL 1	Sets all bits to 1.
	ALL GUARD	Guard key for the above.
	PAGE 0	Sets the bits of 1 page to 0.
	PAGE 1	Sets the bits of 1 page to 1.
⑦	BIT	Programmable pattern setting keys and display lamps
⑧	OUTPUT	Output connectors
	DATA	Data output connector
	$\overline{\text{DATA}}$	Inverse data output connector
	CLOCK1	Clock output connector (Amplitude, offset, and delay can be varied.)
	$\overline{\text{CLOCK1}}$	Inverse clock output connector (Amplitude, offset, and delay can be varied.)
	CLOCK2	Clock output connector (Amplitude, offset, and delay are fixed.)
⑨	CLOCK1	Clock 1 output parameter setting knobs and displays
	DELAY TIME	Clock 1 output (CLOCK1/$\overline{\text{CLOCK1}}$) delay setting knob and display
	BUSY	Display lamp during delay setting
	AMPLITUDE	Clock 1 output (CLOCK1/$\overline{\text{CLOCK1}}$) amplitude setting knob and display
	OFFSET	Clock 1 output (CLOCK1/$\overline{\text{CLOCK1}}$) offset voltage setting knob and display

Table 3-1 Panel Control Explanation (Cont.)

No.	Label	Function
⑩	$\overline{\text{DATA}}$	Inverse data output parameter setting knobs and displays
	AMPLITUDE	Inverse data output amplitude setting knob and display
	OFFSET	Inverse data output offset voltage setting knob and display
⑪	DATA	Data output parameter setting knobs and displays
	AMPLITUDE	Data output amplitude setting knob and display
	OFFSET	Data output offset voltage setting knob and display
⑫	DATA/$\overline{\text{DATA}}$ TRACKING	Data output parameter and inverse data output parameter tracking key
⑬	DISPLAY	Key which switches the data output and clock output parameter setting knob and display between 1/1 SPEED output (front panel outut) and 1/4 SPEED output (rear panel output)
⑭	OFFSET	Offset reference value selector key
⑮	MARK RATIO	Pseudorandom-pattern mark ratio selector keys
⑯	ERROR ADDITION (1×10^{-N})	Error addition amount selector keys and display lamps
⑰	PRBS	Pseudorandom-pattern period (2^N-1) and mark radio display lamps
⑱	≪ ≫	Programmable-pattern data mode, word mode, and pseudorandom-pattern period (2^N-1) selector keys

Table 3-1 Panel Control Explanation (Cont.)

No.	Label	Function
⑲	PROGRAMMABLE PATTERN	Programmable pattern setting
	DATA LENGTH/ NUMBER OF WORD	Data length in data mode and number of words in word mode setting keys and display
	WORD LENGTH	Number of words in word mode setting keys and display
	PAGE	Pattern page specification keys and display; pattern set by ⑦BIT
⑳	PRGM	Programmable pattern mode display lamps
㉑	LOGIC POS/NEG	Output logic positive/negative switch and display lamps
㉒	RESOLUTION MHz/kHz	Frequency setting resolution switch
㉓	FREQUENCY	Internal clock frequency display
㉔	≪ ≫	Frequency change step switch
㉕	TUNING	Frequency setting function ON/OFF switch and display lamp
㉖	◯	Frequency setting knob

Table 3-1 Panel Control Explanation (Cont.)

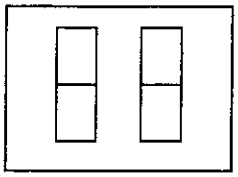
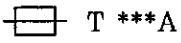
No.	Label	Function
㉗	MEMORY	Patterns and other set conditions memory
	EXIST	Lamp which shows that a registered file exists.
		File number and error code display
		File number setting keys
	DIR/FILE No.	Above file-number-setting-key function selector key and display lamp
	RECALL/ DELETE	Memory contents recall or memory contents delete (shift mode) key and display lamp
	SAVE/RESAVE	Save and resave (shift mode) to file key and display lamp
	SHIFT	Shift mode switch and display lamp
	MODE PTN/OTHERS	Selector key between pattern and other set condition memory functions and display lamp
㉘		Floppy disk drive
㉙	STD 10 MHz	Internal synthesizer reference signal input/output
	BUFFER OUTPUT	Reference signal buffered output connector
	INPUT TTL	Reference signal input connector
	OUTPUT TTL	Reference signal output connector
	INT/EXT	Reference signal oscillator internal/external selector switch

Table 3-1 Panel Control Explanation (Cont.)

No.	Label	Function
㉚	GP-IB	GP-IB connector and address setting switches
㉛	FUNCTION	Function selector switches
㉜	ERROR ADDITION CH (1-32)	Error addition channel selector switches
㉝		U-link for internal synthesizer reference signal OUTPUT/INPUT connector connection
㉞	1/8 SPEED	External pattern inputs and external pattern generation clock output
	CLOCK OUTPUT	External pattern generation clock output connector
	EXTERNAL DATA INPUT	External pattern input connectors and display lamps
	CH SELECT EXT/INT	External pattern/internal pattern selector switches
㉟	AC ** V,  T ***A	Power inlet
㊱		Frame ground terminal
㊲	1/2 CLOCK OUTPUT	1/2 clock output connector
㊳	1/4 SPEED OUTPUT	1/4 clock output connector and 1/4 data output connectors
	CLOCK	1/4 clock output connector
	DATA1	1/4 data 1 output connector
	DATA2	1/4 data 2 output connector
	DATA3	1/4 data 3 output connector
	DATA4	1/4 data 4 output connector

Note : After changing the setting conditions, wait 2 minutes before turning the power OFF.

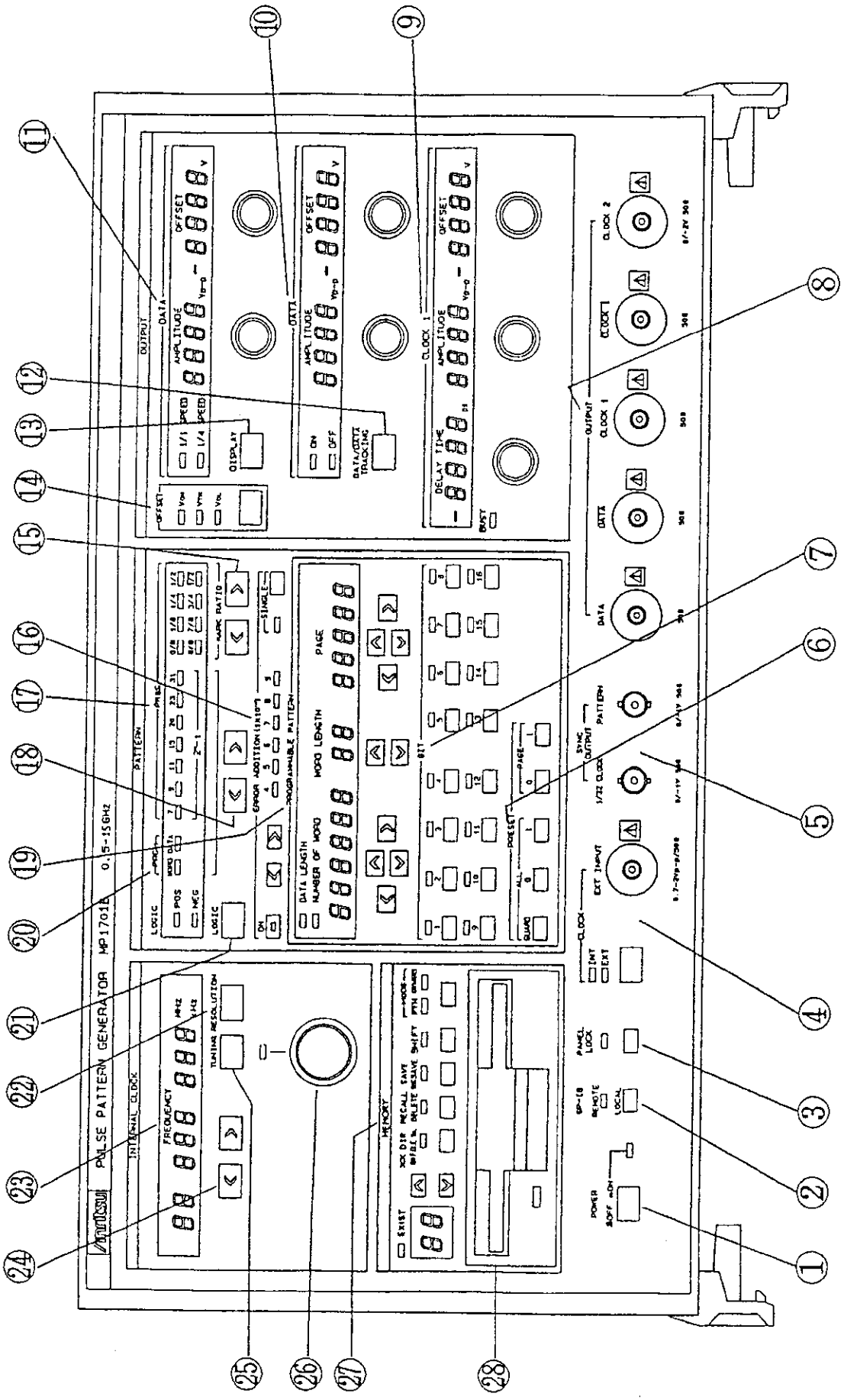


Fig. 3-1 Front panel

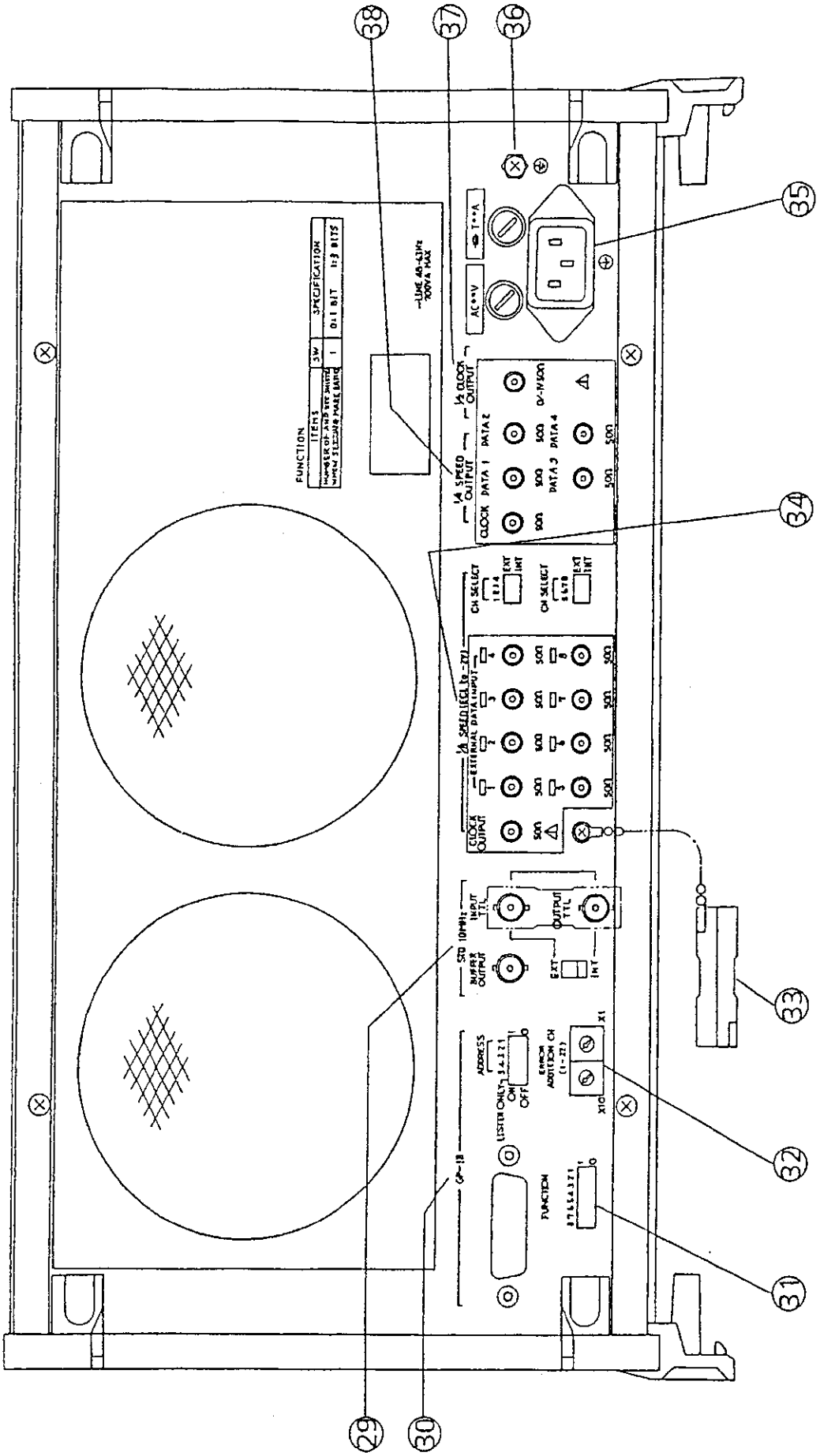


Fig. 3-2 Front panel

SECTION 4

BASIC OPERATION

This section describes the basic operating method and the basic functions of the instrument for those who are using the MP1701B Pulse Pattern Generator for the first time.

Read this section before reading the detailed operating instructions of SECTION 5. Those who have used the MP1601A/MP1604A Pulse Pattern Generator may skip this section.

The number (5), (8), etc. in the text correspond to the controls of Figs. 3-1 and 3-2.

4.1 Setup

To understand the basic operation of the MP1701B, observe its output waveform with a sampling oscilloscope.

Set up the equipment as follows while referring to Fig. 4-1.

Step	Procedure
1	Connect the sampling oscilloscope and MP1701B frame ground terminals to a ground wire. Then, connect the sampling oscilloscope and MP1701B power cords to the AC line and connect the MP1701B to the sampling oscilloscope with coaxial cables.
2	After shorting the shield and internal conductors of the accessory semirigid cables with a piece of metal, connect the DATA and the CLOCK1 output connectors (8) to the sampling oscilloscope channel 1 and channel 2 via. 20 dB pad (att.), respectively.
3	Connect the PATTERN SYNC OUTPUT (5) to the sampling oscilloscope sync input connector.
4	Connect the MP1701B and sampling oscilloscope power cords to an AC outlet. (Use a 3-pole plug with ground and connect it to a grounded outlet. If using a 2-pole plug, connect the sampling oscilloscope and MP1701B frame ground terminals to ground before connecting them to the AC outlet.)

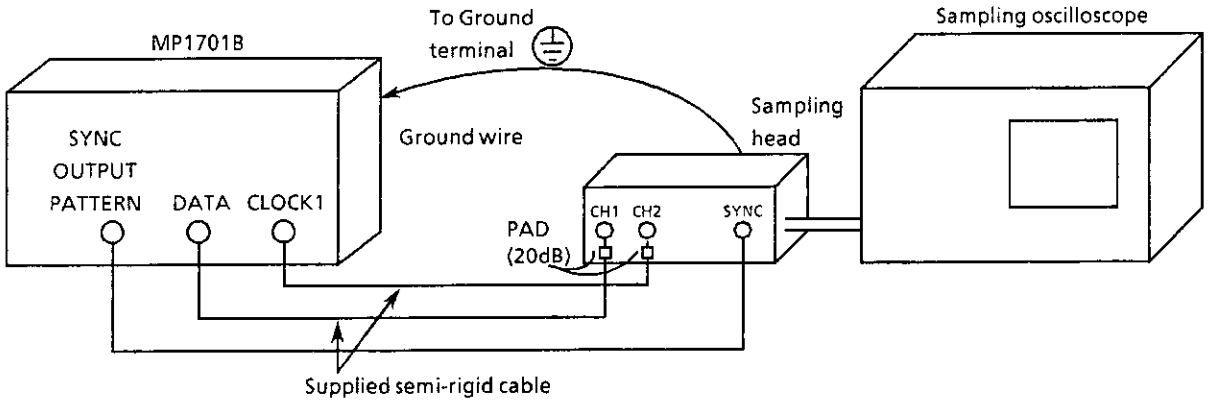
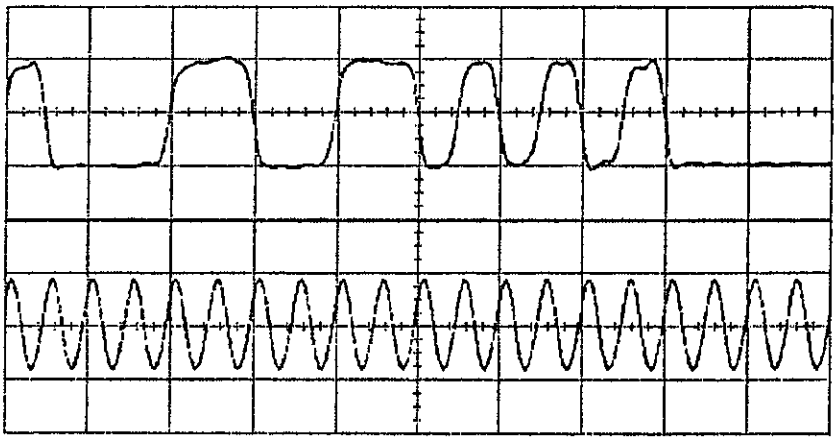


Fig. 4-1 Setup



H: 200 ps/div, Top: DATA
V: 1 V/div, Bottom: CLOCK1
Freq: 10 GHz

Fig. 4-2 DATA and CLOCK1 Waveforms

4.2 Power-On and Operation

Note: When the following operations are performed, the existing memory contents are cleared and are preset to the factory setting state (paragraph 5.12). Check with the previous user to see if there are any patterns that must not be cleared.

Step	Procedure
1	While pressing [LOCAL] (2), turn on the POWER switch (1) . (This operation presets the MP1701B to the factory setting state. When only the power is turned on without pressing [LOCAL], the MP1701B restores the previous setting state.)
2	Press the pattern select key (18) to set PRBS 2^7-1. Adjust the sampling oscilloscope trigger level to synchronize the waveform display as shown in Fig. 4-2. Adjust the sampling oscilloscope delay to check if this pulse pattern is obtained.
3	Press the pattern select key (18) to set to PRGM (Programmable Pattern) DATA (data mode).
4	Press PROGRAMMABLE PATTERN (19)DATA LENGTH [∨] and [∧] to set the data length to 16 bits.
5	Press the BIT keys (7) to set an arbitrary pattern for each 16 bits, and check by comparing the key settings to the waveform on the sampling oscilloscope.
6	Change the frequency as follows. Set the frequency with the TUNING knob (26) after pressing the [TUNING] (25) .
7	After fixing at a suitable frequency, set the data output amplitude and offset by means of the DATA display and its setting knobs (11) . Compare the sampling oscilloscope waveform with the set values.
8	Set the CLOCK1 amplitude, offset, and delay by means of the CLOCK1 display and its setting knobs (9) . Compare the sampling oscilloscope waveform with the set values.

(Blank)

SECTION 5
DETAILED OPERATING INSTRUCTIONS

This section describes the control panel detailed operation and setup methods. Those who want to learn the basic functions of the MP1701B should read SECTION 4 "Basic Operation" before performing actual operation.

5.1 Internal-Clock-Generator Frequency Setting

(1) Frequency setting state

Press the [TUNING] (25) to set the MP1701B to the frequency setting state. (Display lamp lights)

(2) Resolution setting

Press [RESOLUTION] to set the frequency setting resolution to 1 kHz or 1 MHz.

Switching the setting resolution does not affect the frequency setting response time or C/N (SSB phase noise). When the resolution is sufficient at 1 MHz, the unnecessary digits are masked and keeps the compatibility with the conventional MP1601A (5 GHz)/MP1604A (3 GHz) PPG.

(3) Frequency change step setting

Set the frequency change step width with the frequency change step setting keys [<] [>] (24).

When [<] is pressed, the blinking cursor showing the changeable digit of the frequency display (23) moves to the left. When [>] is pressed, it moves to the right.

(4) Frequency setting

Set the frequency by turning the frequency setting knob (26).

5.2 Internal-Clock-Generator Reference Signal Setting

(1) When internal reference generator used

Normally set to this state.

Set the rear panel STD 10 MHz (29) INT/EXT switch to the INT position, and connect the reference signal input connector (INPUT TTL) to the reference signal output connector (OUTPUT TTL) with the U-link (33) .

(2) When external reference generator used

Set the rear panel STD 10 MHz (29) INT/EXT switch to the EXT position, and connect an external reference signal generator to the reference signal input connector (INPUT TTL). The input level is TTL level.

5.3 Word Pattern Setting

(1) Pattern selection

Select the output pattern with [<] and [>] (18) so that the PRGM-WORD lamp (20) lights.

(2) Number of words and word length

When the number of bits making up one word is represented by word length N, and the number of words making up one period is represented by M, the pattern shown in Fig. 5-1 is obtained.

The number of words M setting keys and display are NUMBER OF WORD (19).

The word length N setting keys and display are WORD LENGTH (19).

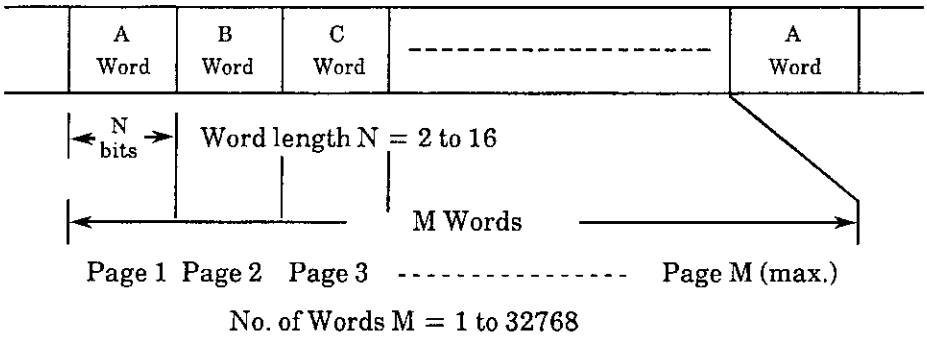


Fig. 5-1 Word-Mode Programmable Pattern

(3) Number of word setting

Press [<] or [>] (19) to move the blinking cursor showing the changeable digit of the number oHowever, the word length and number of words which can be obtained may be restricted. The numbers which can be set conform to Table 5-1.

Note: When the blinking cursor is moved past the left or right end with [<] or [>] (19), the blinking stops and numbers cannot be set. To perform setting again, blink the cursor at the digit to be changed by pressing [<] or [>].

Table 5-1 Word length and Number of Words

Word length N	Number of words M			
	Range	Step width	Range	Step width
2	1 to 2048	1 step	2112 to 32768	64 step
3	1 to 1365	1 step	1408 to 32768	128 step
4	1 to 1024	1 step	1056 to 32768	32 step
5	1 to 819	1 step	896 to 32768	128 step
6	1 to 682	1 step	704 to 32768	64 step
7	1 to 585	1 step	640 to 32768	128 step
8	1 to 512	1 step	528 to 32768	16 step
9	1 to 455	1 step	512 to 32768	128 step
10	1 to 409	1 step	448 to 32768	64 step
11	1 to 372	1 step	384 to 32768	128 step
12	1 to 341	1 step	352 to 32768	32 step
13	1 to 315	1 step	384 to 32768	128 step
14	1 to 292	1 step	320 to 32768	64 step
15	1 to 273	1 step	384 to 32768	128 step
16	1 to 256	1 step	264 to 32768	8 step

(4) Page and pattern setting

The display and keys of PAGE (19) identify, or enable modification of, each word in a pattern with M number of words.

When the page is specified as 1, the contents of the set A word in Fig. 5-1 are displayed at BIT (7) and the A word can be modified with the BIT keys (7).

When the page is specified as 2, the contents of the B word are displayed and can be modified.

Perform the same operation for the C word, etc.

Page specification up to M is possible.

When the word length is 15 bits, the BIT keys and lamps (7) up to 15 are enabled.

(5) Pattern setting state after number of words and word length changed

The pattern setting state after the number of words and word length were changed is shown in Fig. 5-2 by using an example in which both the number of words M and word length N are 4. This state is shown in Fig. 5-2 (a).

If the number of words is changed from 4 to 3, the D word is cleared and the repetitive pattern of words A, B and C is set (Fig. 5-2 (b)). If the number of words is reset to 4, the D word set previously reappears and becomes the repetition of the A, B, C, and D words (Fig. 5-2 (c)).

Next, word length N is changed from 4 to 3.

At this time, bit 4 of each word is cleared (Fig. 5-2 (d)). When N is set to 4 again, bit 4 of each word set previously is reset (Fig. 5-2 (e)).

Generally, when the number of words is changed to a value smaller than the previously set number of words, the data of the leading page side is preserved and the data of the trailing page side is cleared. For word length, the leading bits are preserved and the trailing bits are cleared. The 16 bit is disabled and the BIT 16 lamp is fixed at off.

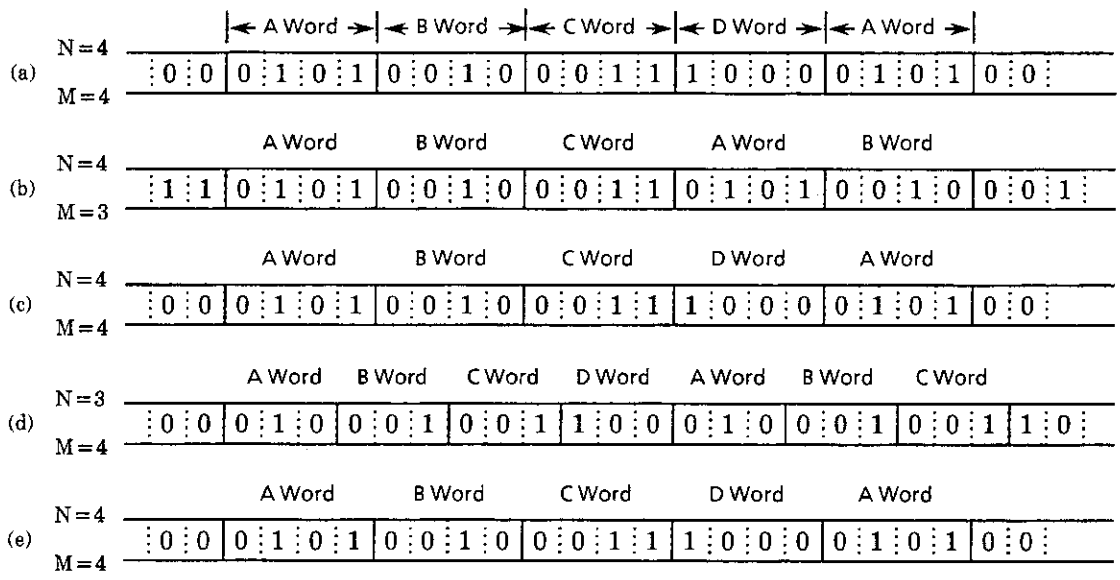


Fig. 5-2 Pattern after Number of Words and Word Length Changed

5.4 Data Pattern Setting

(1) Pattern selection

Select the output pattern to light the PRGM-DATA lamp (20) by pressing [<] and [>] (18) .

(2) Data length setting

In the data mode, if the data length is made N, one period of N bit length pattern is output repeatedly. Set the data length with the PROGRAMMABLE PATTERN (19) DATA LENGTH display, lamp, and keys. The data length can be set from 2 to 524 288 bits. However, when the data length exceeds 4096 bits, setting in 128-bit steps only is possible.

Numbers that are indivisible by 128 cannot be set.

The setting method is the same as that described in paragraph 5.3 (3) "Number of words setting".

(3) Pattern setting

Set the page 1 by pressing the PAGE keys (19).

This allows settings of a pattern of up to bit 16 from the head of the data-length N bits with the BIT keys (7).

When N is smaller than 16, the keys from N + 1 to 16 are disabled and the corresponding lamps remain off.

If N is larger than 16, set to page 2 to set pattern of bit 17 to bit 32. Bits exceeding this can also be set in 16-bit units by specifying page number.

(4) Output pattern when data length changed

When the data length is changed from P to Q, data from the first bit to bit Q is output repeatedly.

If P > Q, since the pattern from bit (Q + 1) to bit P is stored in an internal memory, if the data length is returned to P again, the original pattern is restored and output.epeatedly.

5.5 Programmable Pattern Presetting

(1) All bits "0" setting

Set all bits to "0" by pressing PRESET (6) [ALL 0] while pressing [GUARD].

Note: "All bits" involves the setting bits of the current output pattern and the entire (used and unused) buffer memory contents (512k bits) connected to it.

(2) All bits "1" setting

Set all bits to "1" by pressing PRESET (6) [ALL 1] while pressing [GUARD].

(3) One page "0" setting

Set all the bits of the currently displayed page to "0" by pressing the PRESET (6) [PAGE 0].

Only the settable bits are set to "0". (For instance, when the number of words is 15, bit 1 to bit 15 are set to "0".)

(4) One page "1" setting

Set all the bits of the currently displayed page to "1" by pressing the PRESET (6) [PAGE 1].

Only the settable bits are set to "1".

5.6 Pseudorandom Pattern Setting

(1) Pseudorandom (PRBS) pattern length selection

Press [<] and [>] (18) to select PRBS pattern type.

The bit length of one PRBS pattern period can be selected from among seven bit-lengths from 2^7-1 to 2^{31}-1 bits (2^N-1: N = 7, 9, 11, 15, 20, 23, 31).

(2) Mark ratio selection

Press [<] and [>] (15) to select a PRBS mark ratio of 0/8, 1/8, 1/4, or 1/2.

Select a mark ratio of 8/8, 7/8, 3/4, or $\overline{1/2}$ by inverting the logic by pressing [LOGIC] (21).

(3) Selection of number of AND bit shifts for mark ratio 1/8, 1/4, 7/8, and 3/4 pattern generation

Select the number of AND bit shifts at mark ratio 1/8, 1/4, 7/8, and 3/4 pattern generation as 1 bit or 3 bits by switching rear panel FUNCTION switch 1 (31). (For details, see paragraph 6.4)

Table 5-2 Number of AND Bit Shifts Selection

FUNCTION switch 1	No. of AND bit shifts
0	1 bit
1	3 bits

5.7 Logic Inversion

(1) Programmable-pattern logic

The BIT (7) lamps, when lit, indicate "1". When off, they indicate "0". When the POS lamp is lit to select positive logic by pressing [LOGIC] (21), "1" corresponds to high level output and "0" corresponds to low level output. When the NEG lamp is lit to select negative logic, "1" corresponds to low level output and "0" corresponds to high level output.

(2) Pseudorandom-pattern logic

For pseudorandom pattern, for positive logic, "1" corresponds to low level output and "0" corresponds to high level output (see block diagram at Table 6-1).

5.8 Error Addition

Step	Procedure
1	Press the ERROR ADDITION (16) [ON]. (The lamp lights.)
2	Select the error addition rate by pressing [<] and [>] (16). For single error addition, on bit error is added each time [SINGLE] is pressed.
3	Select the channel at which error is to be added with the rear panel ERROR ADDITION CH (1-32) switches X10 and X1 (32). (The left switch (X10) sets the tens digits and the right switch (X1) sets the units digit. 01 to 32 can be set. When 00 is set, error is added at CH1 and when 33 to 99 is set, error is added at CH32.)

Note: When the output pattern is divided into each bit as shown in Fig. 5-3, the bit at which error is to be added is selected with these switches X1 and X10.

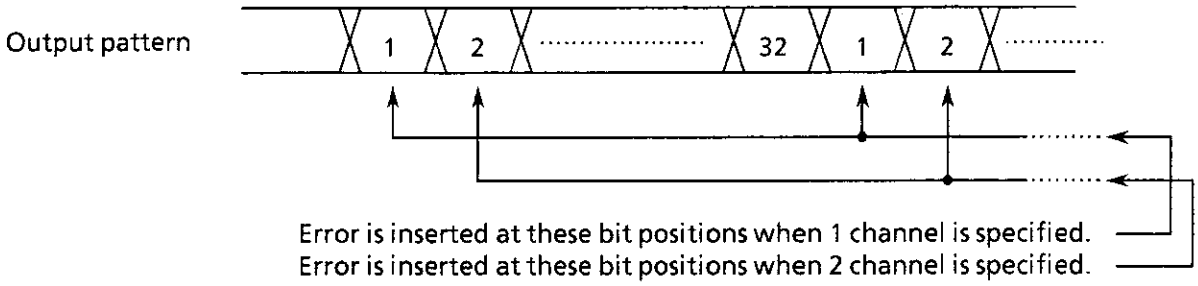


Fig. 5-3 Error Addition Channel

5.9 Output Amplitude, Offset Voltage, and Delay Setting

(1) DATA, $\overline{\text{DATA}}$, CLOCK1, $\overline{\text{CLOCK1}}$

Light the 1/1 SPEED lamp by pressing [DISPLAY] (13). Turn the $\overline{\text{DATA}}$ (11), DATA (10), and CLOCK1 (9) setting knobs to set the amplitude, offset voltage, and CLOCK1 delay.

(2) DATA, $\overline{\text{DATA}}$ tracking function

Turn on the tracking function by pressing [DATA/$\overline{\text{DATA}}$ TRACKING] (12). The $\overline{\text{DATA}}$ (10) setting knobs are disabled and the display goes off.

The $\overline{\text{DATA}}$ output amplitude and offset voltage are automatically made the same values as DATA output.

When the DATA (11) amplitude and offset voltage setting knobs are turned in this state, both the DATA and $\overline{\text{DATA}}$ output amplitudes and offset voltages are changed simultaneously.

(3) 1/4 CLOCK, 1/4 DATA

Light the 1/4 SPEED lamp by pressing [DISPLAY] (13).

Set the 1/4 DATA amplitude and offset voltage with the DATA (11) setting knobs, and the 1/4 CLOCK amplitude and offset voltage with the CLOCK (9) setting knobs.

At this time, the $\overline{\text{DATA}}$ (10) amplitude, offset voltage, and $\overline{\text{CLOCK1}}$ delay setting knobs are disabled and the display goes off.

(4) Offset-reference-value selecting function

Set the DATA (11), $\overline{\text{DATA}}$ (10), and CLOCK1 (9) offset voltage reference values to V_{OH} (output high level), V_{TH} (center level between output high and low levels), or V_{OL} (output low level) by selecting V_{OH}, V_{TH}, or V_{OL} with [OFFSET] (14).

The output levels (when the amplitude is changed by switching the offset reference value) are shown in Fig. 5-4.

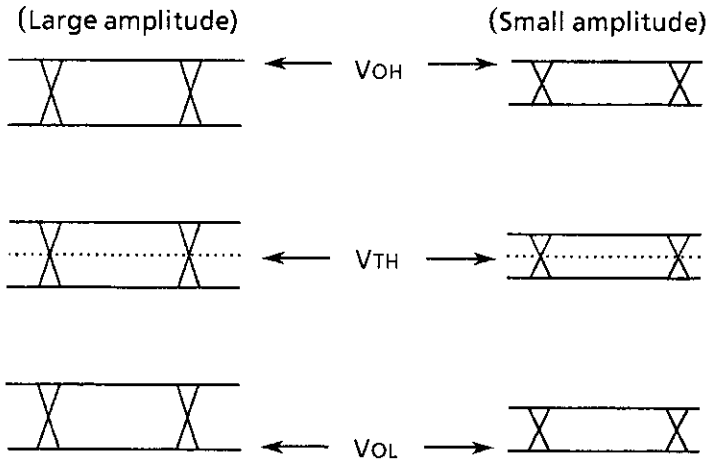


Fig. 5-4 Offset Reference Value and Amplitude Change

Note: Since the offset-voltage upper and lower limit values are limited by V_{OH} (-2.0 V $\leqq$ V_{OH} $\leqq$ +2.0 V), when V_{TH} or V_{OL} are set, the amplitude is limited at a certain value and may not change further.

Example: If V_{OL} is set at +1.00 V offset voltage and if there is a signal with amplitude 0.5 Vp-p added, that amplitude can only be increased to 1.0 Vp-p.

This is because their superposition after the increase would be meeting the maximum allowable level +2.00 V.

Figures 5-5 to 5-10 show the relationships between amplitude and offset-voltage settable ranges at three offset references.

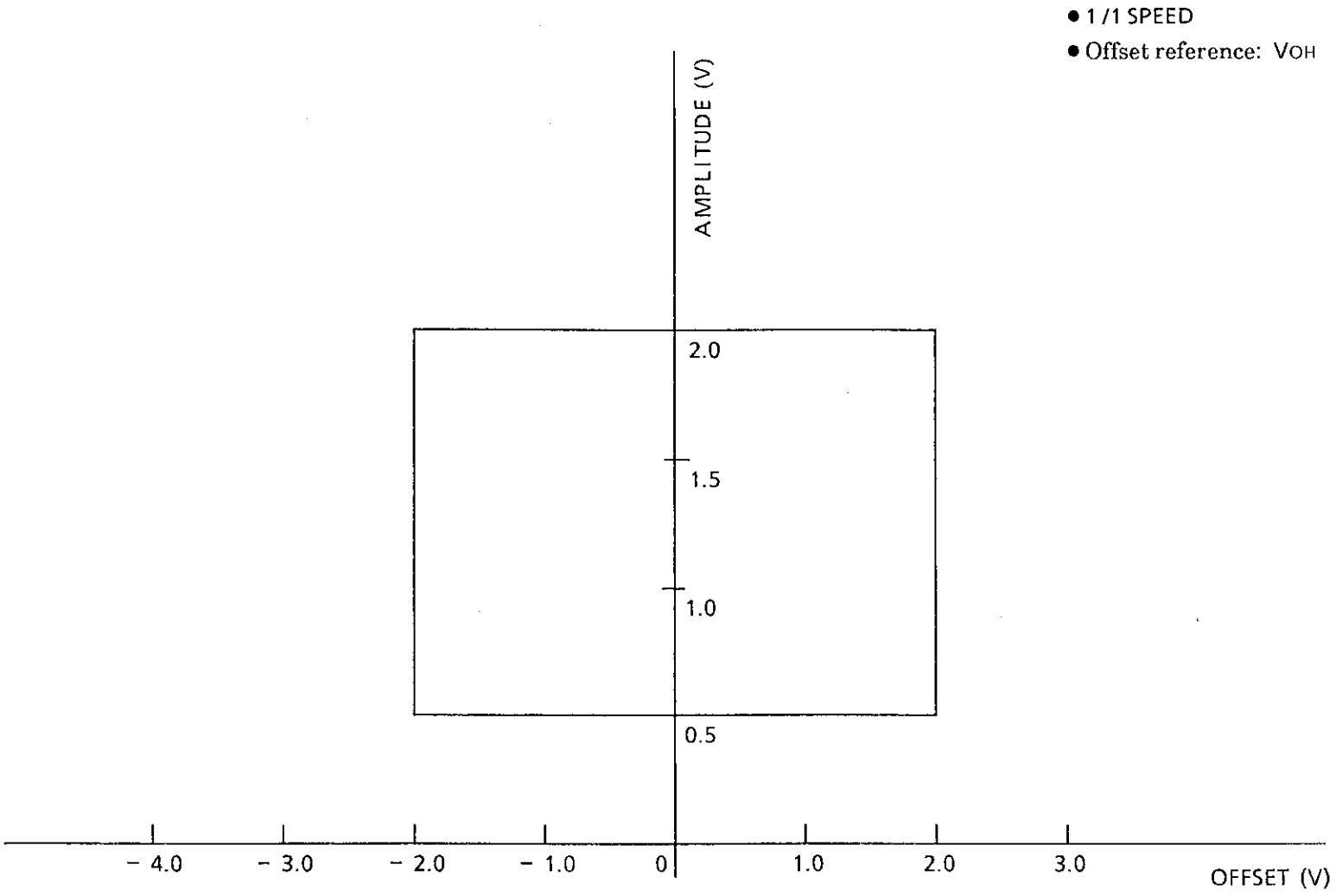


Fig. 5-5 Amplitude and Offset Voltage Setting Range Corresponding to Offset Reference Value

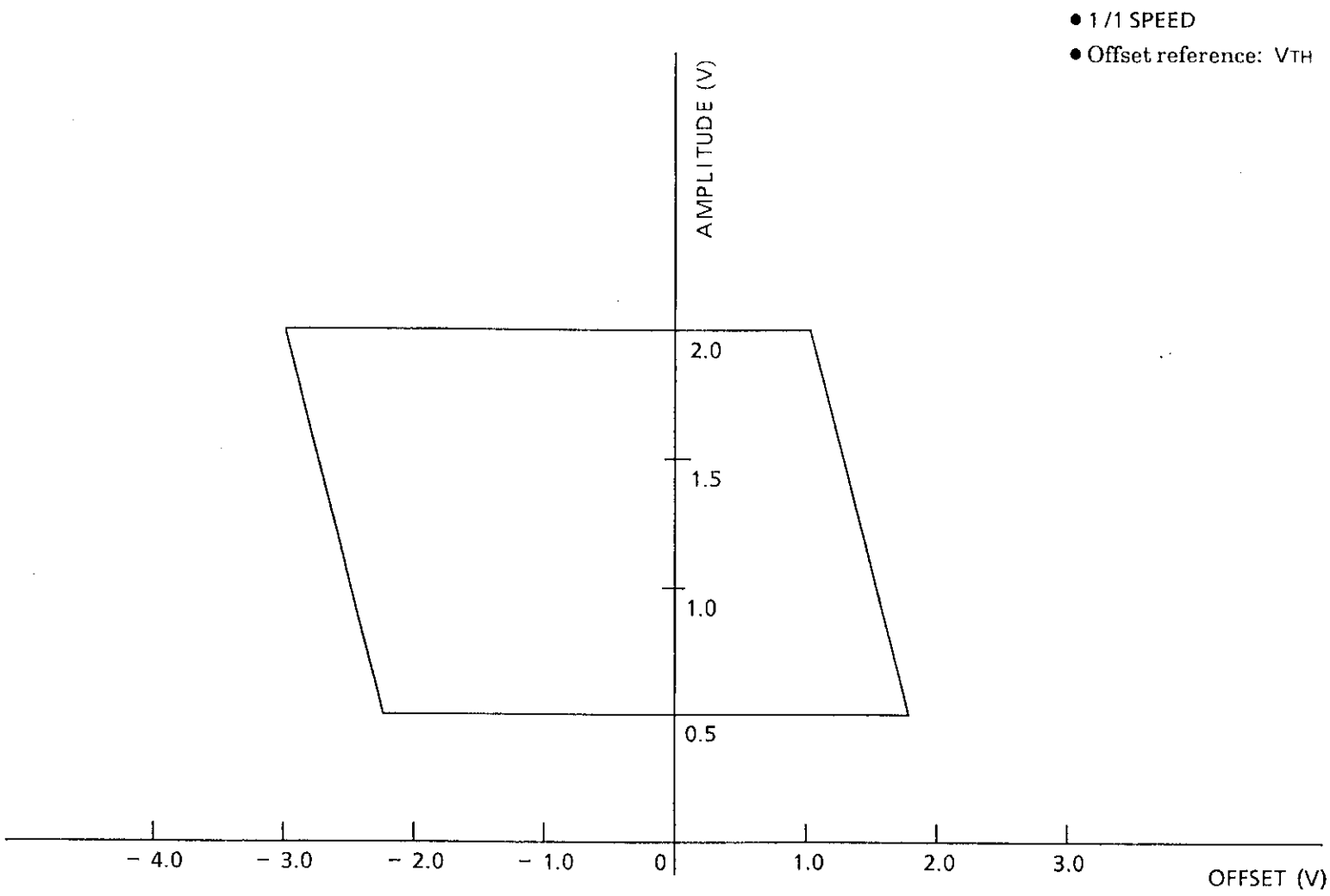


Fig. 5-6 Amplitude and Offset Voltage Setting Range Corresponding to Offset Reference Value

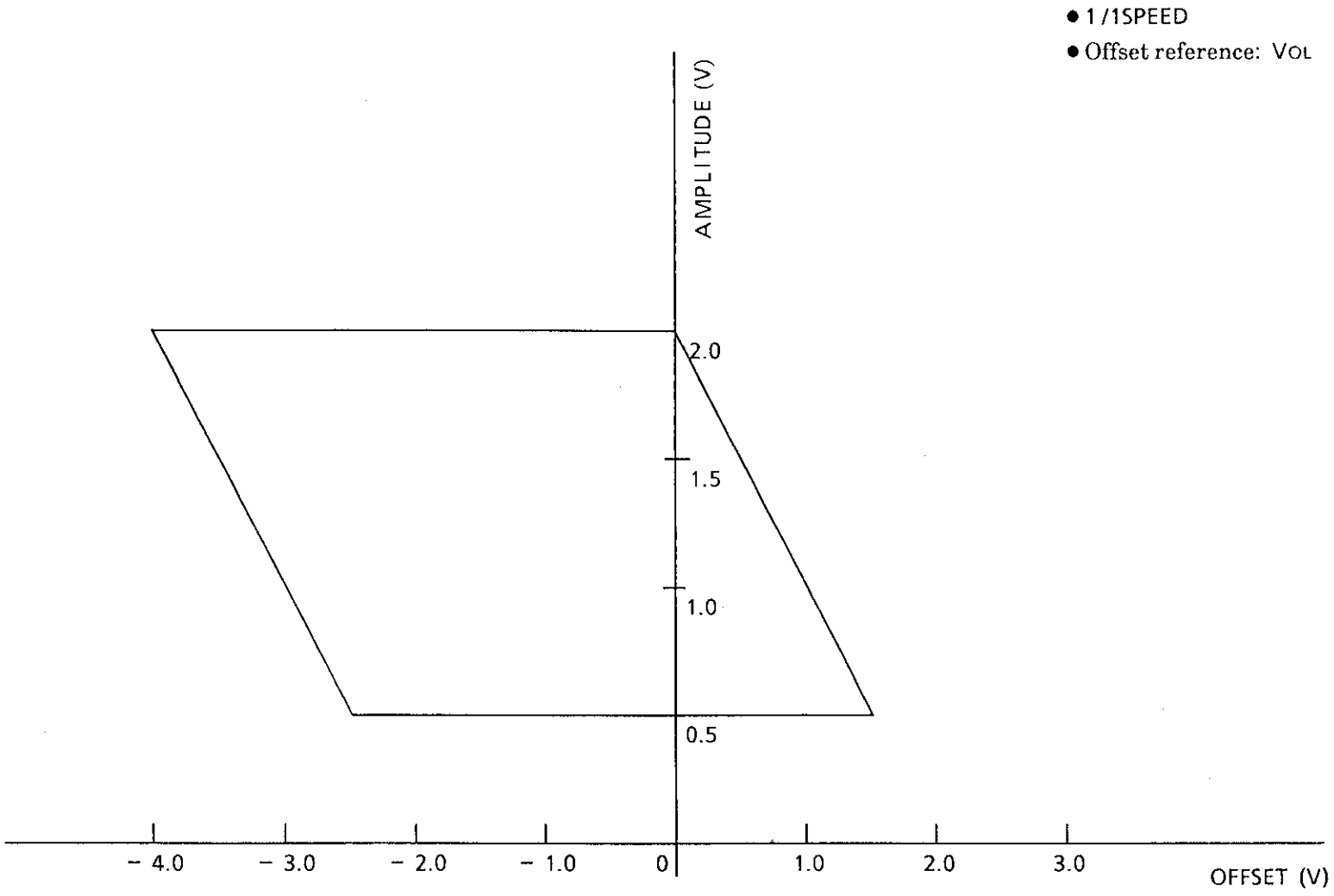


Fig. 5-7 Amplitude and Offset Voltage Setting Range Corresponding to Offset Reference Value

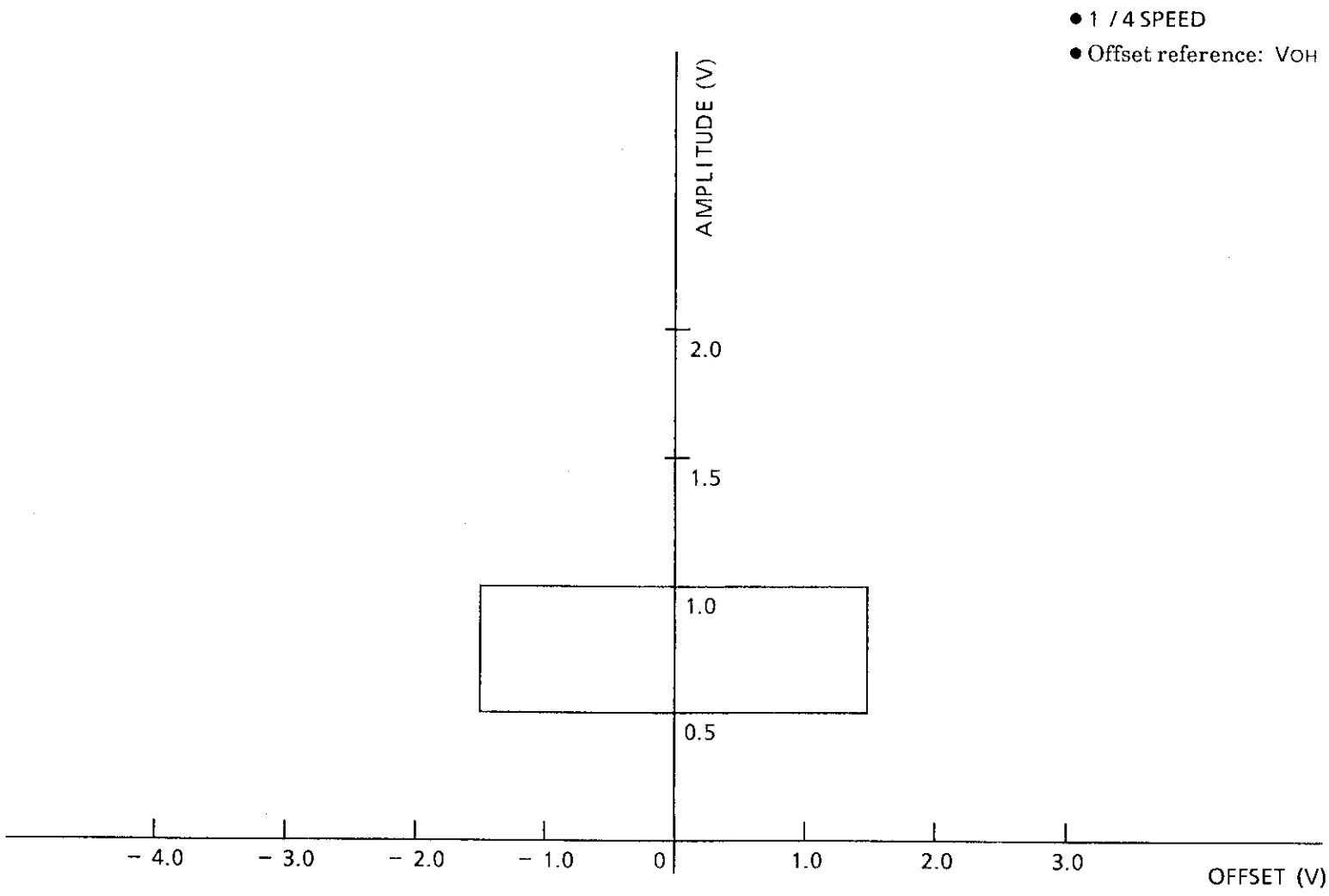


Fig. 5-8 Amplitude and Offset Voltage Setting Range Corresponding to Offset Reference Value

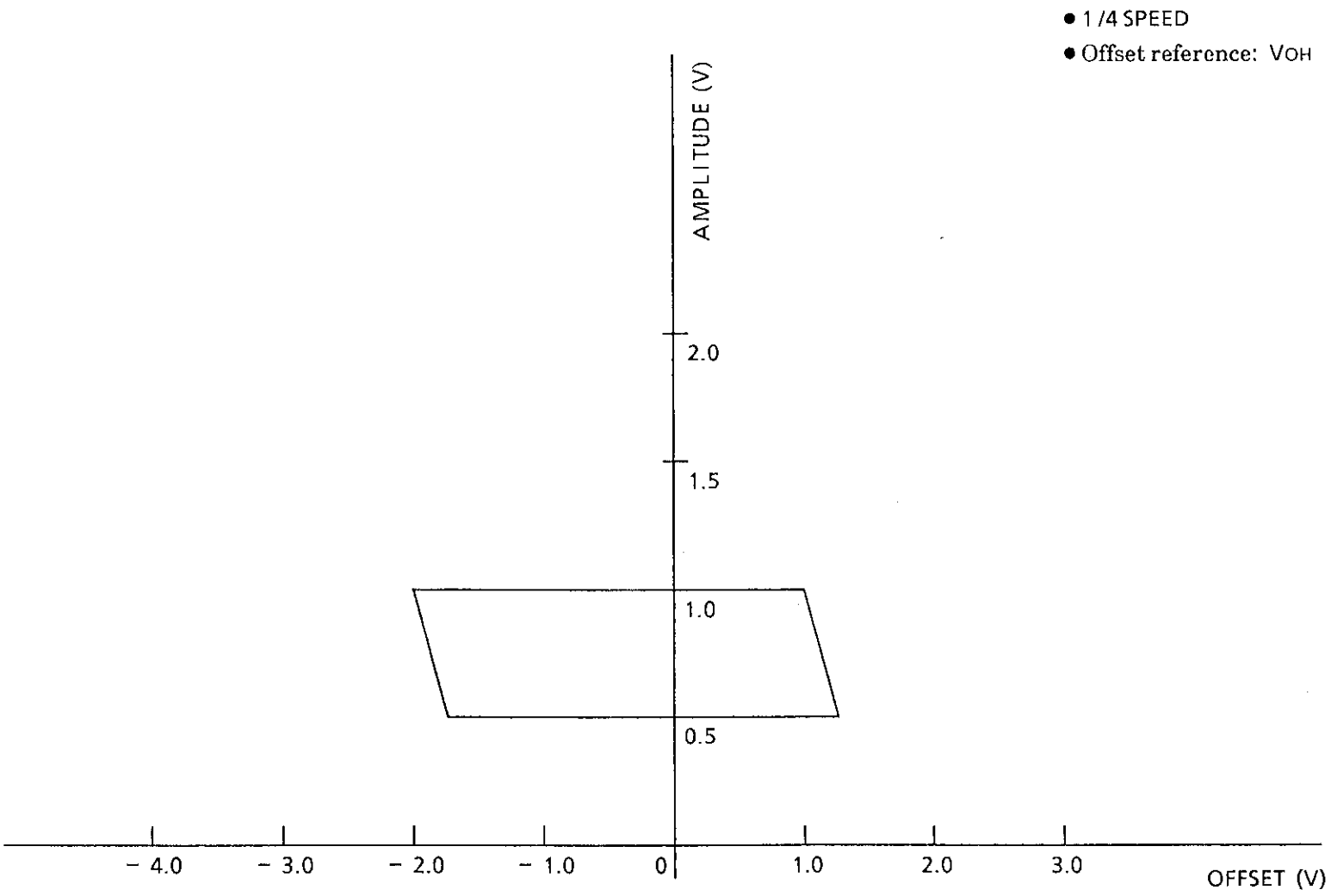


Fig. 5-9 Amplitude and Offset Voltage Setting Range Corresponding to Offset Reference Value

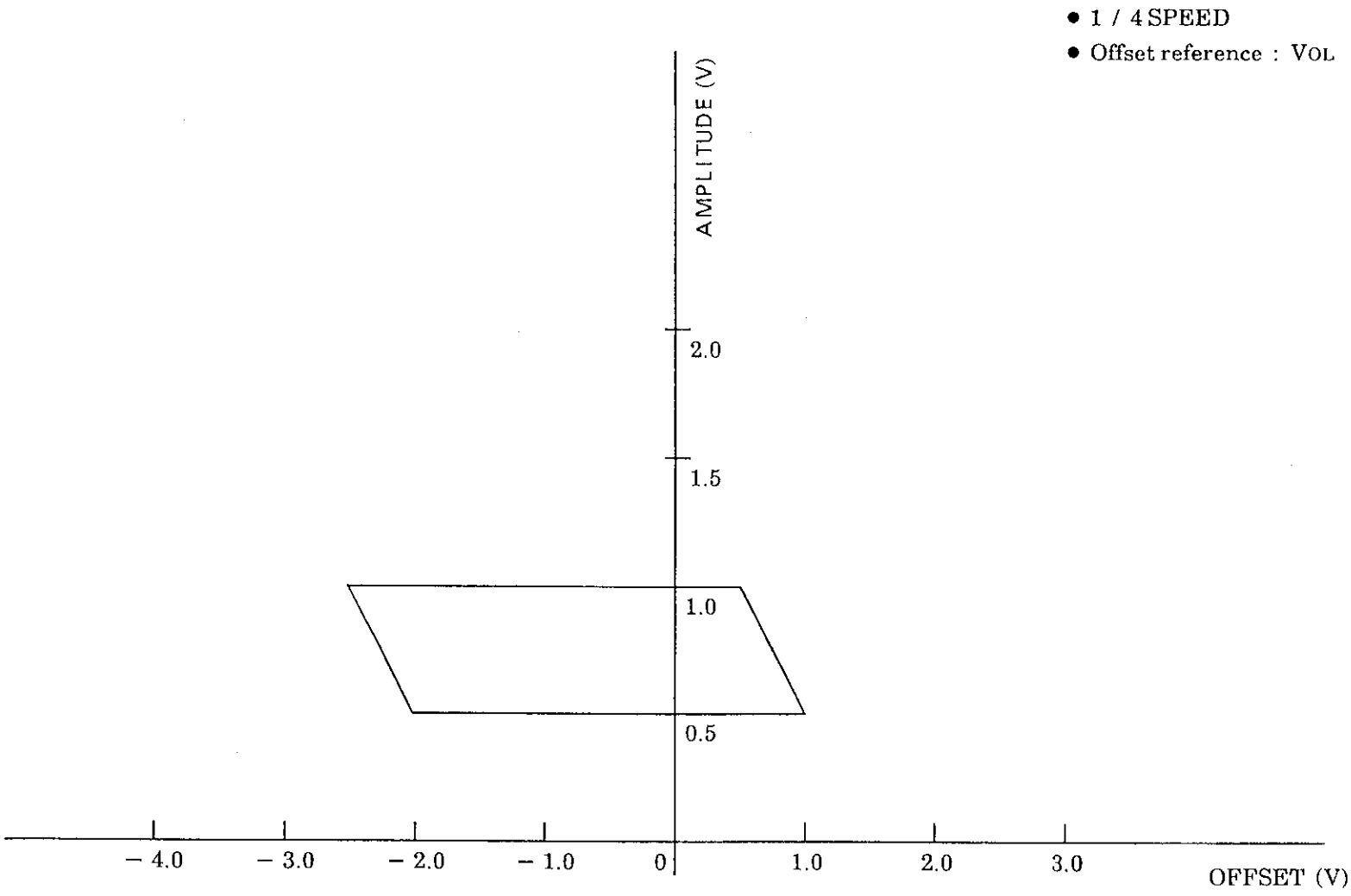


Fig. 5-10 Amplitude and Offset Voltage Setting Range Corresponding to Offset Reference Value

5.10 Memory

(1) Floppy disk insertion

Insert a formatted 3.5-inch 2HD-type floppy disk into the floppy disk drive (28) . (The accessory floppy disk is formatted. For the formatting method, see paragraph 5.10 (8).)

(2) Mode setting

Set the PTN (pattern) mode or OTHERS mode by pressing MEMORY (27) . [MODE PTN/ OTHERS]. In the PTN mode, the pattern set contents are stored; in the OTHERS mode, other set conditions (frequency, amplitude, offset voltage, etc.) are stored.

For each mode, file names from 00 to 99 can be selected.

(3) File save

Select the FILE No. display mode by pressing [DIR/FILE No.]. Select the desired file name (00 to 99) by pressing [∧] or [∨] and then press [SAVE]. In the PTN mode, the pattern set contents are saved; in the OTHERS mode, the other set conditions are saved.

(4) File recall

Select the PTN mode or OTHERS mode, and select the desired file name by pressing [∧] or [∨].

Press [RECALL] to recall the contents of the file.

(5) Directory

Select the DIR mode with [DIR/FILE No.] to access the floppy disk and check the saved file. Press [∧] or [∨] to display only the names of the exist files on the inserted floppy disk. When there are no files on the inserted floppy disk, "——" is displayed.

In the DIR mode, recall, resave, and delete operations can be performed, but the save operation cannot be performed.

When returned to the FILE No. mode from the DIR mode, and if the file set with [∧] or [∨] exists, the EXIST lamp lights.

Note: When the floppy disk is changed after the DIR mode is set, set the DIR mode again.

This is because the read directory information is stored in the MP1701B even if the floppy disk is removed and the directory information will not match when a different floppy disk is inserted.

(6) File resave

After setting the shift mode by pressing [SHIFT], press [RESAVE] to resave an existing file.

However, resave may be impossible, depending on the free storage capacity of the floppy disk. Read the resave operation described in paragraph 5.10 (12).

(7) File delete

After setting the shift mode by pressing [SHIFT], press [DELETE] to delete an existing file.

(8) Floppy disk formatting

Set the OTHERS mode and FILE No. mode, then press [∧] to display Fr (Fr follows 99).

After pressing [SHIFT], press [DELETE] to format the floppy disk.

It takes about two minutes to format a floppy disk.

(9) Error message

When a floppy disk error occurs, error code E0 to E9 is displayed on the file name display.

The error messages are shown in Table 5-3.

All the keys in the MEMORY section, other than [∨] and [∧], are disabled during error message display. To reset the error display, press [∨] and [∧] once.

Table 5-3 Error Messages

Error item	Error contents
E0	Media error (formatting or media error)
E1	Write protection error
E2	File full (insufficient write area)
E3	File not found (specified file not found at read)
E4	File exists error (save of same file is attempted)
E5	Write error
E6	Read error
E7	File type, file error (file type or file contents error)
E8	FD error (other error)
E9	Hardware error (hardware trouble error)

(10) Memory capacity

Usually, 200 files can be stored on one floppy disk; 100 files in the OTHERS mode and 100 files in the PTN mode. However, when long data length and word length patterns are stored, the number of files that can be stored may decrease.

For example, when 512k bit patterns are stored, only 18 files can be stored (paragraph 5.10(11)(e)).

(11) Floppy disk

(a) Disk type

The floppy disk is formatted in standard MS-DOS format provided by the MS-DOS file handler. The formatted floppy disk becomes data disk type. This is because the MS-DOS handler does not copy the MS-DOS system.

The system disk containing the MS-DOS system can also be used to store data.

(b) Volume label

The volume label is provided when the floppy disk is formatted.

Volume label: MP1701A_DAT

This volume label is used to identify the floppy disk.

(c) File configuration

- Directory configuration

  The directory configuration is root directory only.

- File name, extension

  The file name and extension have the format shown below.

PTN: Pattern file
OTH: Parameter file for other than pattern

Examples: T99. PTN
T01. OTH

(d) Data format

Since the format of the data stored in floppy disk is not, as a rule, open to the user; operation is not guaranteed when data is generated, modified, etc.by using a personal computer that operates under MS-DOS.

However, file directory checking and file copying are no problem.

(e) 512k bits pattern data and floppy disk capacity

As mentioned previously inparagraph 5.10(10), for 512k bits pattern data, only 18 files can be stored.

The directory is shown below.

```
T99          PTN          65640     89-11-14   13 : 13
T98          PTN          65640     89-11-14   13 : 13
T97          PTN          65640     89-11-14   13 : 14
T96          PTN          65640     89-11-14   13 : 14
T95          PTN          65640     89-11-14   13 : 15
T94          PTN          65640     89-11-14   13 : 15
T93          PTN          65640     89-11-14   13 : 16
T92          PTN          65640     89-11-14   13 : 16
T91          PTN          65640     89-11-14   13 : 17
T90          PTN          65640     89-11-14   13 : 17
T89          PTN          65640     89-11-14   13 : 18
T88          PTN          65640     89-11-14   13 : 19
T87          PTN          65640     89-11-14   13 : 19
T86          PTN          65640     89-11-14   13 : 20
T85          PTN          65640     89-11-14   13 : 20
T84          PTN          65640     89-11-14   13 : 21
T83          PTN          65640     89-11-14   13 : 22
T82          PTN          65640     89-11-14   13 : 22
```

Note: Refer to paragraph 5.10 (12).

(f) Actual stored data

The dump list of the data stored on a floppy disk is shown below. This data is for DATA pattern, data length = 512.

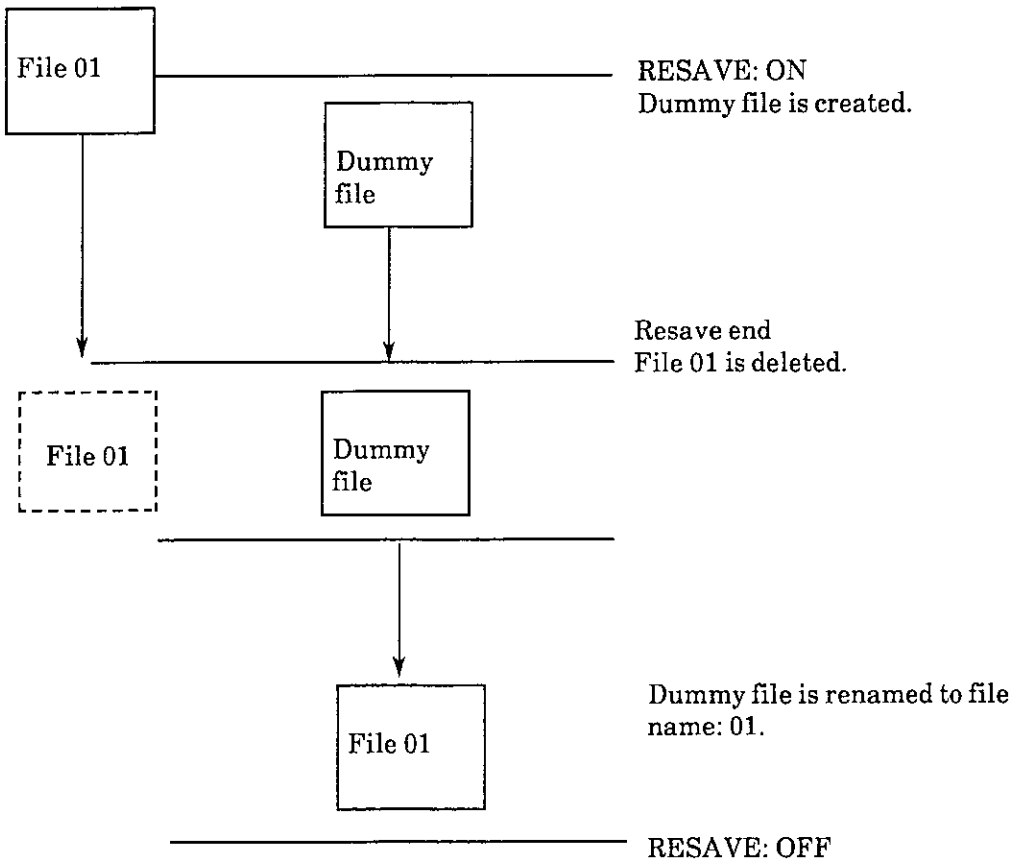
Dump Version 2.1.

```
00000000    00 00 00 00 31 2E 30 20-00 00 00 00 00 00 00 01
00000010    00 00 00 01 00 00 00 00-00 00 00 05 00 00 80 00
00000020    00 00 00 06 00 01 86 A0-00 00 00 10 00 00 00 02
00000030    00 00 00 01 00 00 00 06-00 00 00 01 00 00 00 01
00000040    00 00 00 01 00 00 02 00-00 00 00 01 00 00 00 01
00000050    00 00 00 20 00 00 00 01-00 00 00 03 00 00 00 01
00000060    00 00 00 20 00 00 00 01-00 01 00 02 00 04 00 08
00000070    00 10 00 20 00 40 00 80-01 00 02 00 04 00 08 01
00000080    10 00 20 00 40 00 7F FF-80 00 C0 00 E0 00 F0 01
00000090    F8 00 F0 00 FE 00 FF 00-FF 80 FF C0 FF E0 FF F0
000000A0    FF F8 FF FC FF FE FF FF-00 00 00 00 00 00 00 00
```

(12) Resave operation

The resave function performed by the MP1701B is shown below.

When file named 01 is resaved, the following operation sequence is performed.



Resave cannot be performed by the operation above if the free space on the floppy disk is not equal to, or greater than, the size of the file to be resaved.

That is, for paragraph 5.10 (11) (e), since the free space on the floppy disk is only 52 224 bytes, a 65 640-byte file cannot be resaved.

(13) Key operation during floppy disk accessing

While the floppy disk is accessed in the following operations,

- SAVE
- RESAVE
- RECALL
- DELETE
- FORMATTING
- DIRECTORY SEARCH

keys and knobs are almost in the same condition as panel lock and remain in the locked state up to the end of access.

(14) Notes on floppy-disk handling

Please pay careful attention to the following points.

- Do not remove the floppy disk from equipment being accessed.
- Observe the specified environmental conditions. Also, do not use the equipment in a dusty place.
- Keep magnetic objects away from the disk. Do not bend the disk.
- Insert the head protection sheet into the disk slot when moving the equiment.
- Files saved via the MP1701B Pulse Pattern Generator cannot be loaded into the MP1702A or any other instrument.

5.11 External Pattern Input

The MP1701B can be used as an 8:1 multiplexer by inputting external patterns to the rear 1/8 SPEED EXTERNAL DATA INPUT connector (34). An example is shown in Fig. 5-11.

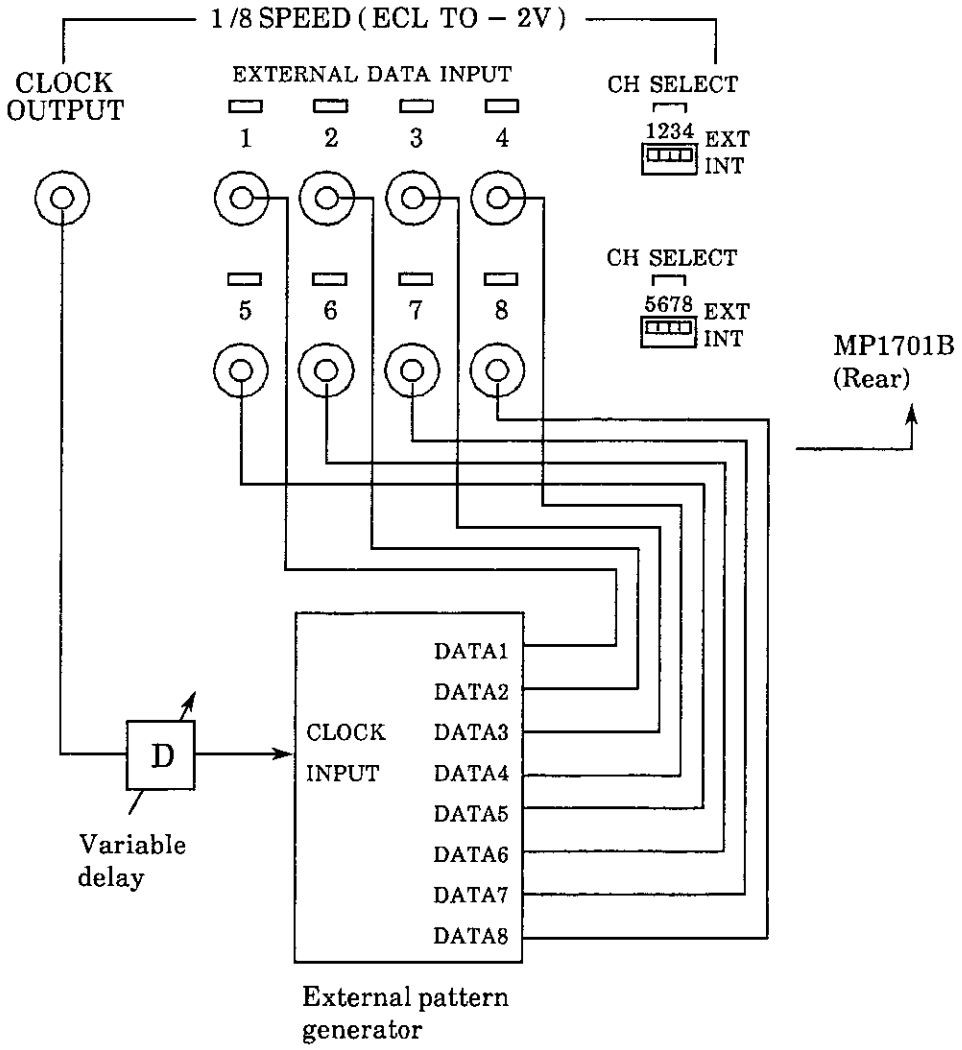


Fig. 5-11 External Pattern Input Setup

Set the CH SELECT switch of the channel to be input from the outside, to the EXT position.

The input level is ECL level (50 Ω, −2 V termination).

The relation between external input data and final output is shown in Fig. 5-12. Match the phases of the external input data as shown in Fig. 5-13.

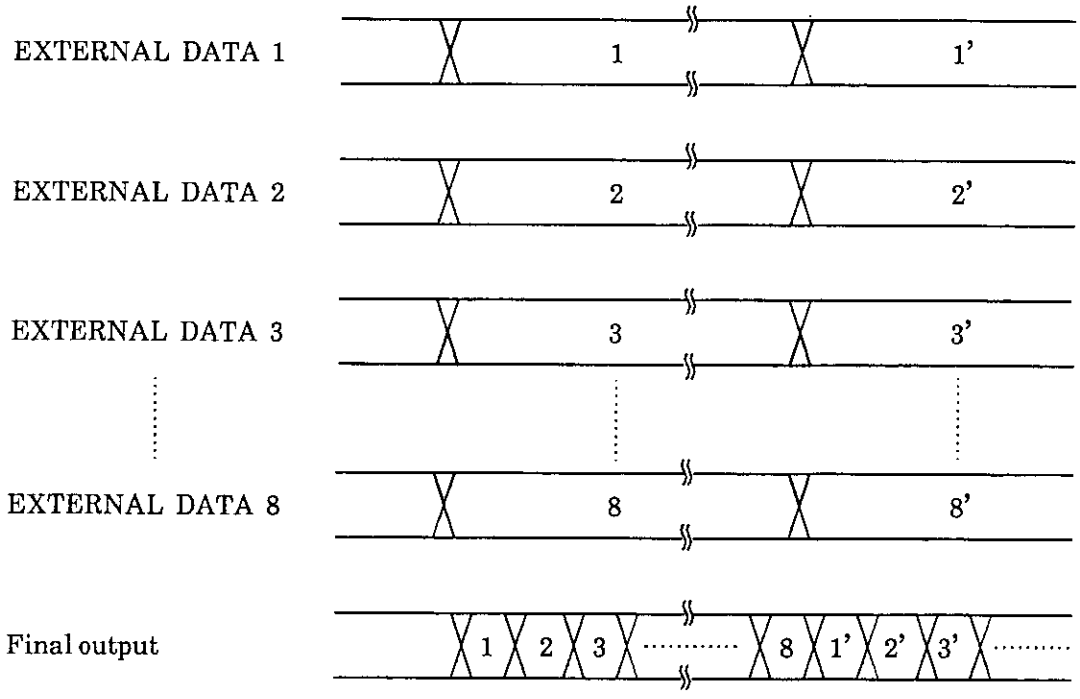
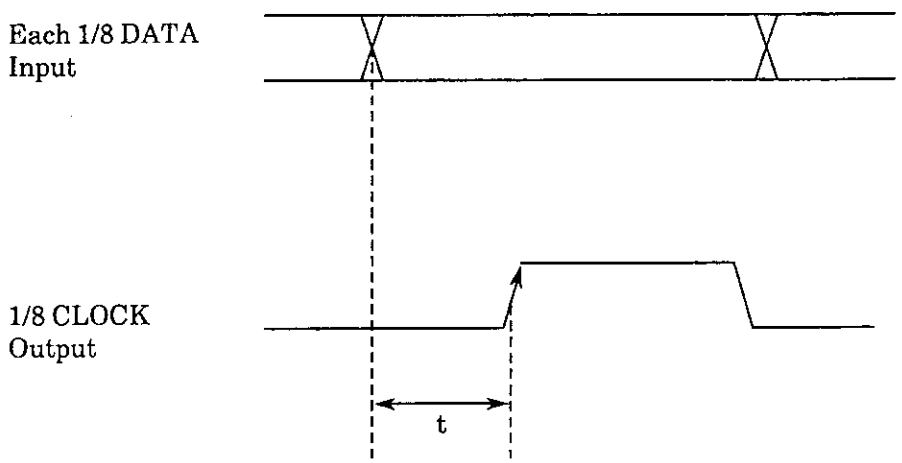


Fig. 5-12 External Input Data and Final Output



$$(9.6 - \frac{8\times10^9}{f})\text{ns} \leqq t \leqq 9.2\,\text{ns}$$

f: Fundamental clock frequency [Hz]

Fig. 5-13 External Pattern Input Data Phase Matching

5.12 Parameters Initialization

When desiring to set the pattern type, amplitude, offset voltage, and other setting conditions to the factory-settings, turn on the POWER switch #1 while pressing [LOCAL] #2.

This initializes the settings. The initial state is shown in Table 5-4,

Table 5-4 Initial State

Item	Initial setting
CLOCK	INT
FREQUENCY	10 000 000 kHz
TUNING	ON
MEMORY	00 (PTN mode, FILE NO. mode)
PATTERN	PRBS $2^{15}-1$
MARK RATIO	1/2
LOGIC	POS
ERROR ADDITION	OFF
OFFSET	V_{OH}
DISPLAY	1/1 SPEED
DATA/$\overline{\text{DATA}}$ TRACKING	OFF
DATA AMPLITUDE	1.000 Vp-p
DATA OFFSET	0.000 V
$\overline{\text{DATA}}$ AMPLITUDE	1.000 Vp-p
$\overline{\text{DATA}}$ OFFSET	0.000 V
CLOCK1 AMPLITUDE	1.000 Vp-p
CLOCK1 OFFSET	0.000 V
CLOCK1 DELAY TIME	0 ps
1/4 DATA AMPLITUDE	1.000 Vp-p
1/4 DATA OFFSET	0.000 V
1/4 CLOCK AMPLITUDE	1.000 Vp-p
1/4 CLOCK OFFSET	0.000 V

(Blank)

SECTION 6
PRINCIPLES OF OPERATION

6.1 Block Diagram

The MP1701B block diagram is shown in Fig. 6-1.

6.2 Internal Clock Generator (A1)

The clock generator is a synthesized clock generator consisting of PLL circuits with a 10 MHz crystal oscillator as the reference signal.

6.3 Programmable Pattern Generator (A8)

The programmable pattern setting data is stored in RAM.

This RAM has 128 outputs. These outputs are multiplexed sequentially at later stages and are finally converted into one serial output.

6.4 Pseudorandom Pattern Generator (A11)

A PRBS generation LSI generates 32 patterns.

These 32 patterns are multiplexed at later stages and are finally converted into one PRBS pattern.

The PRBS pattern generation principle is shown in Table 6-1. The mark ratio 1/4 and 1/8 pattern generation circuit is shown in Fig. 6-2.

Generally, a PRBS pattern with a period of 2^N-1 bits has one N-bit continuous "1" pattern per period.

Since an inverter circuit is inserted at the final stage as shown in Fig. 6-2, when LOGIC is set to POS (positive logic), DATA output "1" corresponds to low level and "0" corresponds to high level.

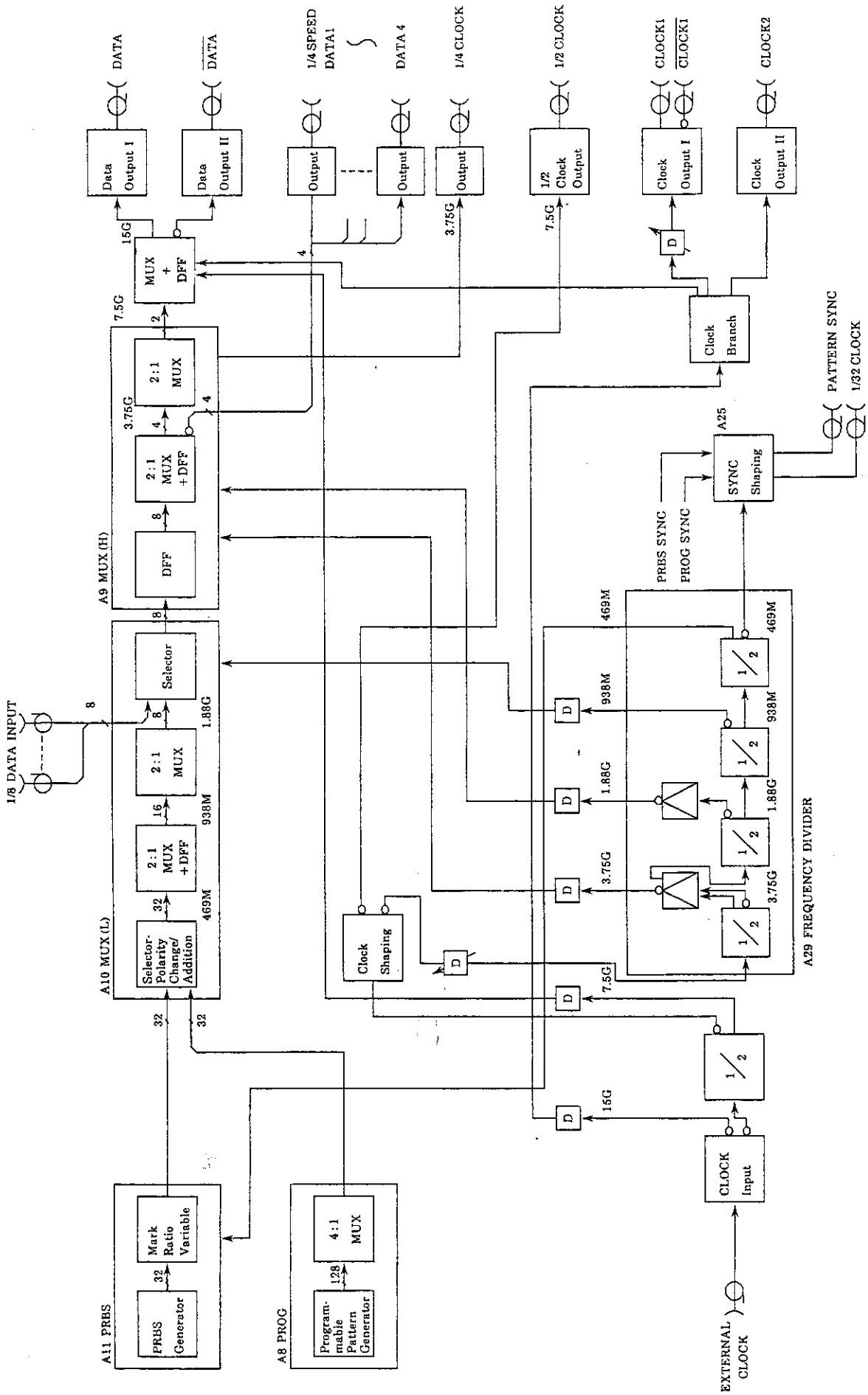


Fig. 6-1 MP1701B Block Diagram

Table 6-1 Pseudorandom Pattern Generation Principle

Period	Generaton polynominal	Pattern Generation Block Diagram
2^7-1	$1+X^6+X^7$	
2^9-1	$1+X^5+X^9$	
$2^{11}-1$	$1+X^9+X^{11}$	
$2^{15}-1$	$1+X^{14}+X^{15}$	
$2^{20}-1$	$1+X^3+X^{20}$	
$2^{23}-1$	$1+X^{18}+X^{23}$	
$2^{31}-1$	$1+X^{28}+X^{31}$	

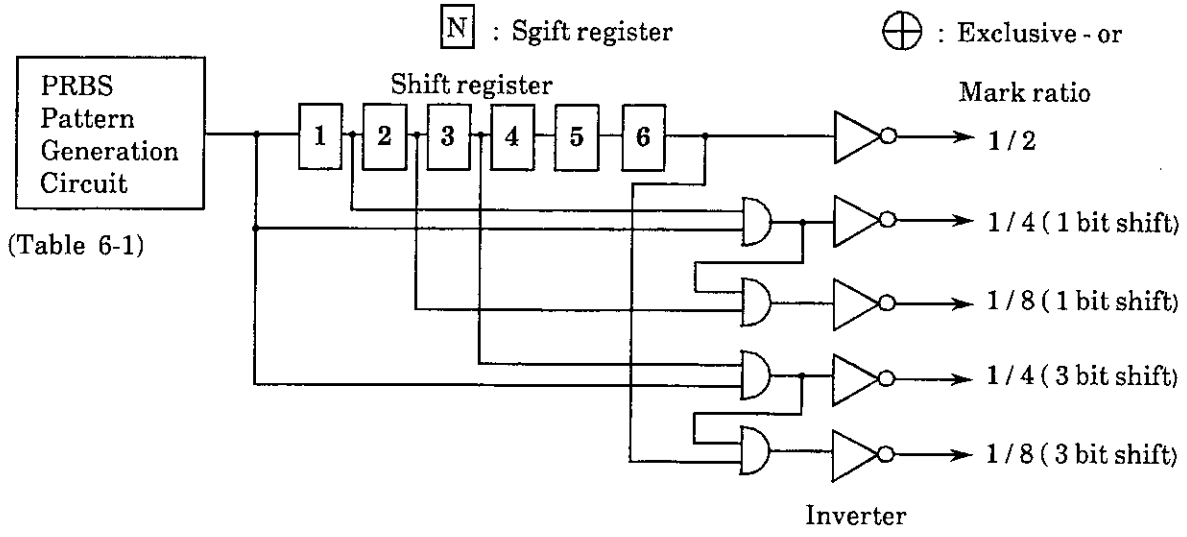


Fig. 6-2 Mark Ratio 1/4, 1/8 Pattern Generator

6.5 Pattern Sync Output Period

6.5.1 Pseudorandom pattern

Period = [1/(set frequency)] × (2^N-1) × 32

N = 7, 9, 11, 15, 20, 23, 31

where, plus pulse with pulse width = [1/(set frequency)] × 32

6.5.2 Programmable pattern

(1) Data mode

(a) When data length is 4096 or less

Period = [1/(set frequency)] × (least common multiple between 128 and data length)

(Examples)

1. When data length is 8.

   Period = [1/(set frequency)] × 128

2. When data length is 10.

   Period = [1/(set frequency)] × 640

(b) When data length exceeds 4096

Period = [1/(set frequency)] × (data length)

(2) Word mode

Because (word length) × (number of words) = data length, the pattern sync output period is the same as that described in paragraph (1) Data mode.

(3) Pulse width

For all the program patterns, the pulse width = [1/(set frequency)] × 64.

The output signal polarity is plus pulse.

6.6 1/4 Data Output and 1/4 Clock Output

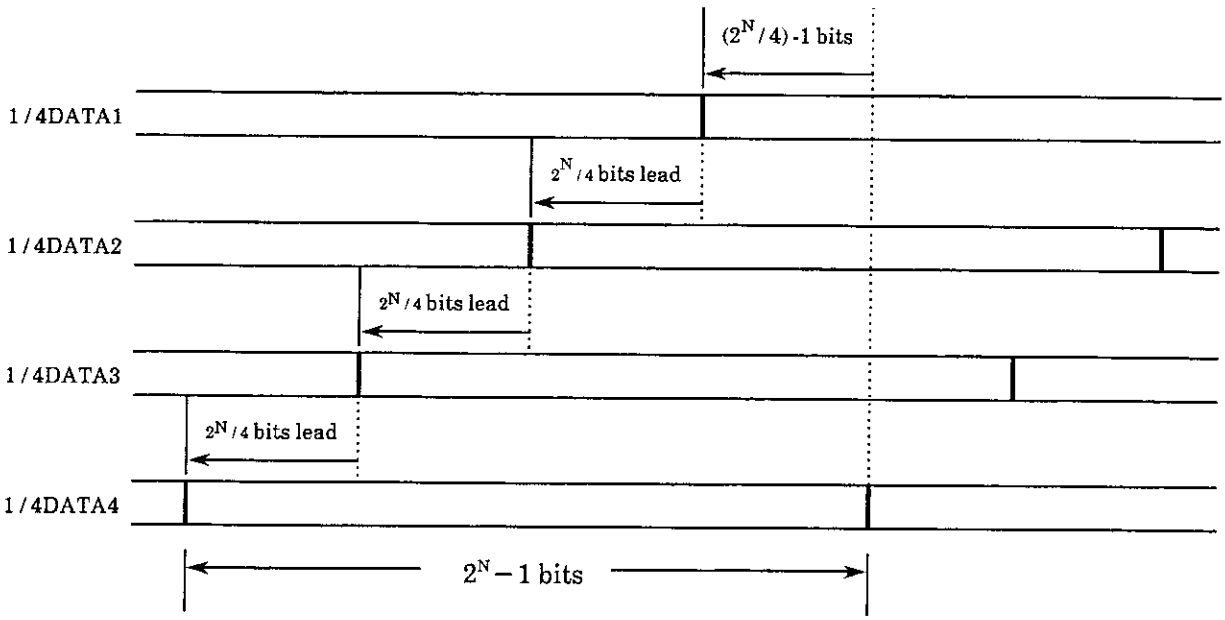
For MUX IC test, etc., a 1/4-speed clock and 4-channel data output are provided. Each data channel signal can be output independently. (However, for the programmable pattern, the maximum capacity per channel is 128k bits.)

The pattern sequence for programmable pattern is shown in Table 6-2. The pattern sequence for the pseudorandom pattern is shown in Fig. 6-3.

Table 6-2 1/4 Data Output Pattern Sequence

DATA output on front panel (Serial)		1 2 3 4	5 6 7 8	9 10 11 12	13 14 15 16	17 18 19 20	21 22 23 24	Max. 524 288 bits
		1 0 0 1	0 1 1 1	0 0 1 1	1 0 1 0	1 1 0 0	0 1 1 1	
Output on rear panel (paral-lel)	1	1	0	0	1	1	0	
	2	0	1	0	0	1	1	
	3	0	1	1	1	0	1	
	4	1	1	1	0	0	1	
		1 bit	2 bit	3 bit	4 bit	5 bit	6 bit	Max. 131 072 bits

Note: The pattern set on the front panel are set every 4 bits for each channel.



Note: $2^N / 4 = 8192$ bits at PRBS 2^{15}-1

Fig. 6-3 Pseudorandom Pattern Sequence

(Blank)

SECTION 7
PERFORMANCE TEST

7.1 Introduction

When performing performance tests at receiving inspection, routine tests, operation check after repair, etc., proceed as described below.

Routine tests should be performed at least once every year.

7.2 Equipment Required

The equipment required to perform the performance tests are shown in Table 7-1.

Table 7-1

No.	Equipment name	Main performance	Test item
1	MF76A Microwave Frequency Counter	10 Hz to 18 GHz	Frequency accuracy
2	MS612A Spectrum Analyzer	Up to 5.5 GHz	SSB phase noise
3	Synthesized signal generator (SG)	Up to 6 GHz SSB phase noise: −90 dBc/Hz or less (at 10 kHz offset)	SSB phase noise.
4	Mixer	RF and LO frequencies: 5 to 10 GHz IF output frequency: 0.4 to 5 GHz	SSB phase noise
5	Sampling oscilloscope	• Normal mode Frequency band: up to 12.4 GHz or 18 GHz Rise time: ≦28.2 ps or ≦19.4 ps • Averaging mode Frequency band: up to 20 GHz or 34 GHz Rise time: ≦17.5 ps or ≦10.3 ps	Amplitude Offset voltage Rise/fall time Waveform distortion, jitter
6	Trigger count down	Up to 18 GHz	Jitter
7	MP1702A Error Detector	50 MHz to 10 GHz	Pattern

7.3 Performance Test

CAUTION: Ground the equipment to be setup (incuding the device under test) and discharge the outer and inner conductors of the cables with a piece of metal before setup (paragraphs 2.5 and 4.1).

7.3.1 Internal clock generator frequency accuracy

(1) Specifications

Frequency accuracy: ≦ ±1 ppm

(2) Setup

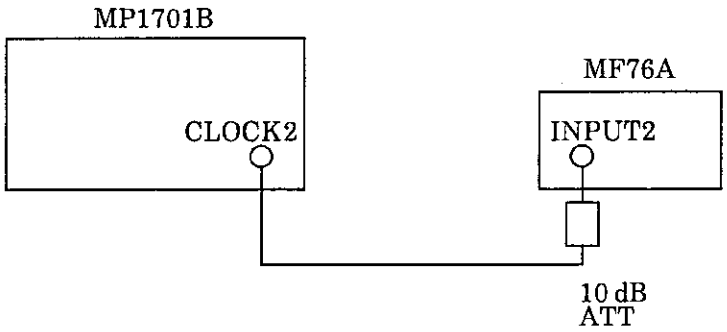


Fig. 7-1 Setup

(3) Procedure

Step	Procedure
1	Set the MP1701B clock selector key (4) to INT.
2	Set the freqency to 10 GHz.
3	Set the MF76A INPUT SELECT to INPUT2.
4	Set the MF76A FUNCTION to MANUAL and input the approximate frequency to be measured (10 GHz here) from the ten key pad.
5	Read the MF76A measured value and compare it to the rating.
6	Change the MP1701B frequency and repeat steps 4 and 5 at each frequency

7.3.2 Internal clock generator SSB phase noise

(1) Specifications

SSB phase noise (10 kHz offset, bandwidth 1 Hz)

- ≦ −85 dBc (<4 GHz)
- ≦ −80 dBc (4 to 8 GHz)
- ≦ −75 dBc (≧8 GHz)

(2) Setup

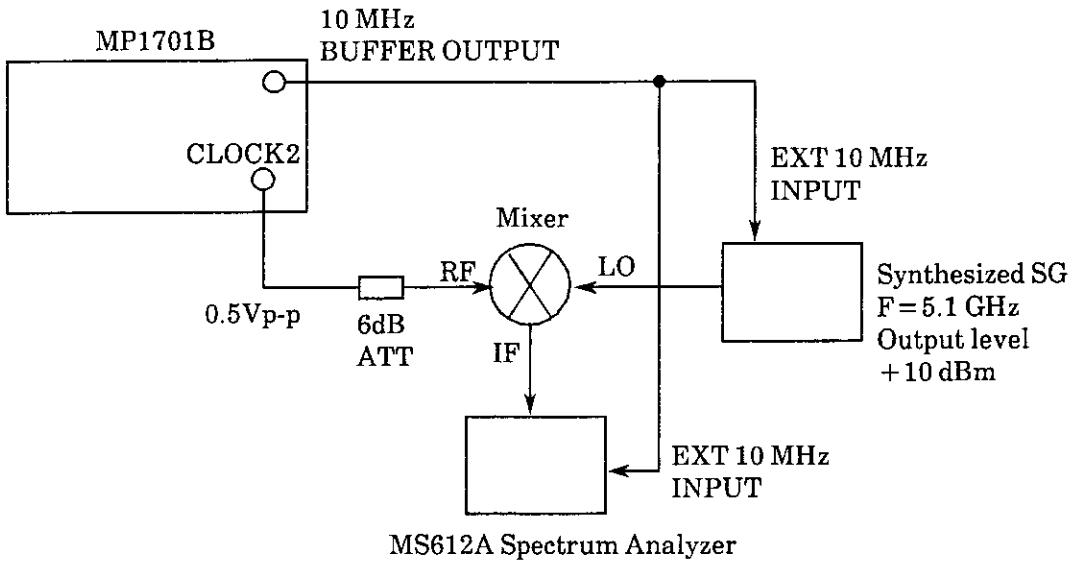


Fig. 7-2 Setup (5.5 GHz to 10 GHz)

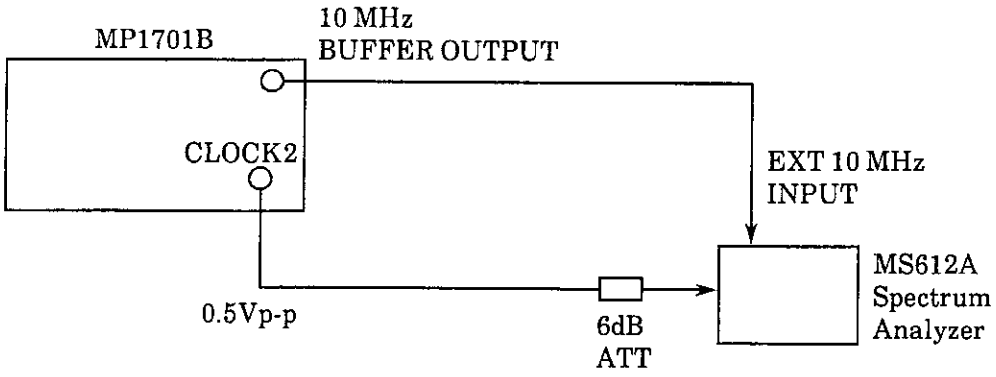


Fig. 7-3 Setup (50 MHz to 5.5 GHz)

(3) Procedure

Step	Procedure
1	Set up the equipment as shown in Fig. 7-2 and set the MP1701B frequency to 10 GHz.
2	Set the synthesized SG frequency to 5.1 GHz.
3	Set the MS612A center frequency to (10 GHz − 5.1 GHz + 10 kHz) = 4.900 01 GHz.
4	Set the MS612A frequency span to 20 kHz, resolution bandwidth (RBW) to 300 Hz, and video bandwidth (VBW) to 10 Hz.
5	Using the marker, read the difference between the levels at 4.900 01 GHz and 4.900 00 GHz using the MS612A. When this level difference is made XdB, the SSB phase noise can be obtained from the following equation: SSB phase noise = $X - 10\log_{10}\left(\frac{300}{\text{RBW}} \times \frac{1.2}{\text{Correction coefficient}}\right) + \underbrace{2.5}_{\text{Correction coefficient}}$ Example: When X = −65dB, SSB phase noise becomes −88.06 dBc/Hz
6	Change the MP1701B frequency and perform the same test. At this time, set the MS612A center frequency based on the following equation: MS612A center frequency = (MP1701B set frequency) − (synthesized SG frequency) + 10 kHz ***Note:*** Select the synthesized SG frequency so that the above center frequency can be set with the MS612A.
7	When testing at 50 MHz to 5.5 GHz, set up the equipment as shown in Fig. 7-3.
8	Read the difference (assumed as X dB) between the levels at (MP1701B set frequency + 10 kHz) and at the MP1701B set frequency, and obtain the SSB phase noise as in step 5.

7.3.3 DATA, $\overline{\text{DATA}}$, 1/4DATA rise and fall times

(1) Specifications

DATA, $\overline{\text{DATA}}$ tr, tf ≦ 30 ps

1/4DATA tr, tf ≦ 200 ps

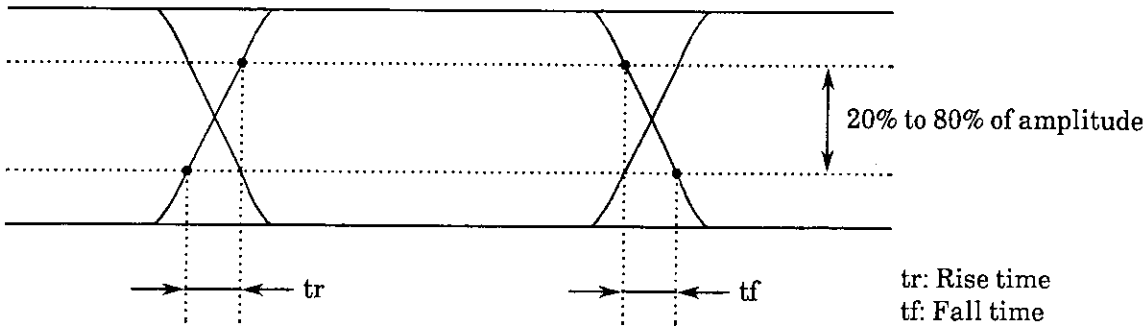


Fig. 7-4 Rise/Fall Time

(2) Setup

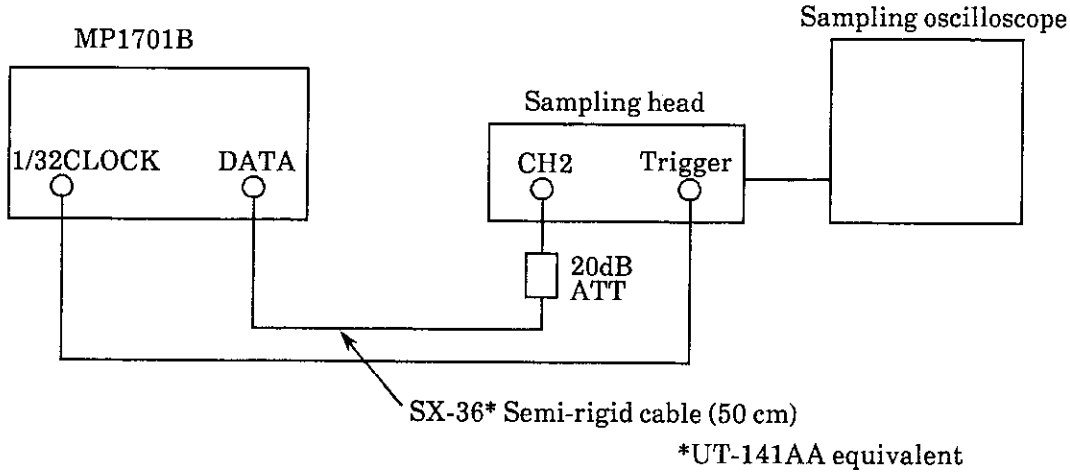


Fig. 7-5 Setup

(3) Procedure

Step	Procedure
1	Adjust the sampling oscilloscope trigger level to synchronize the waveform.
2	Set the MP1701B output pattern to PRBS 2^{15}-1.
3	Measure the DATA tr and tf in accordance with Fig. 7-4.
4	Change the MP1701B frequency, amplitude, and offset voltage, and measure the DATA tr and tf.
5	Change the connection to $\overline{\text{DATA}}$ and measure tr and tf similarly.
6	Change the connection to 1/4DATA1 to 4 and measure each tr and tf similarly.

7.3.4 DATA, $\overline{\text{DATA}}$, 1/4DATA amplitude and offset voltage

(1) Specifications

DATA, $\overline{\text{DATA}}$ amplitude

0.5 to 2 Vp-p, 10 mV steps

Setting error: $\leqq \pm 15\%$ or ± 100 mV, whichever is greater

DATA, $\overline{\text{DATA}}$ offset voltage

-2 to $+2$ V (V_{OH}), 5 mV steps

Setting error: $\leqq \pm 15\%$, ± 100 mV or $\pm 15\%$ of amplitude, whichever is greatest.

1/4DATA amplitude

0.5 to 1 Vp-p, 10 mV steps

Setting error: $\leqq \pm 15\%$ or ± 100 mV, whichever is greater

1/4DATA offset voltage

-1.5 to $+1.5$ V (V_{OH}), 5 mV steps

Setting error: $\leqq \pm 150$ mV

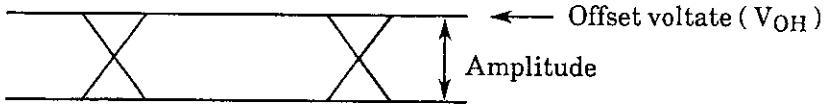


Fig. 7-6 Amplitude and Offset Voltage

(2) Set up

The setup is the same as that inparagraph 7.5.3 (2) and is shown in Fig. 7-5.

(3) Procedure

Step	Procedure
1	Calibrate the sampling oscilloscope vertical axis sensitivity.
2	Adjust the sampling oscilloscope trigger level to synchronize the waveform.
3	Set the MP1701B output pattern to PRBS 2^{15}-1.
4	Set the MP1701B OFFSET reference value to V_{OH}.
5	Measure the DATA amplitude and offset voltage (V_{OH}) in accordance with Fig. 7-6 and check if the error from the set value is within the specifications.
6	Change the connection to $\overline{\text{DATA}}$ and 1/4DATA1 to 4 and check similarly.

7.3.5 DATA, $\overline{\text{DATA}}$ jitter

(1) Specifications

DATA, $\overline{\text{DATA}}$ jitter

≦25 ps

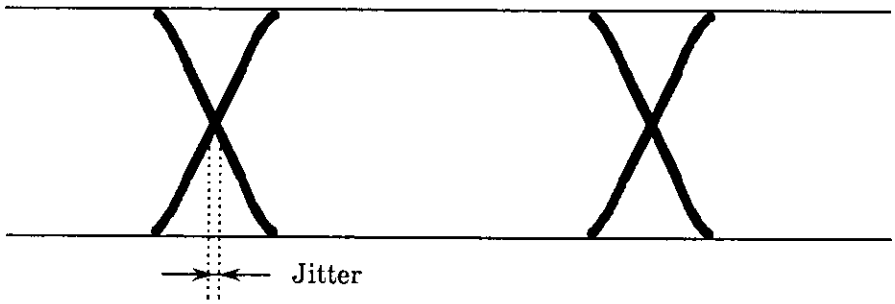


Fig. 7-7 Jitter

(2) Setup

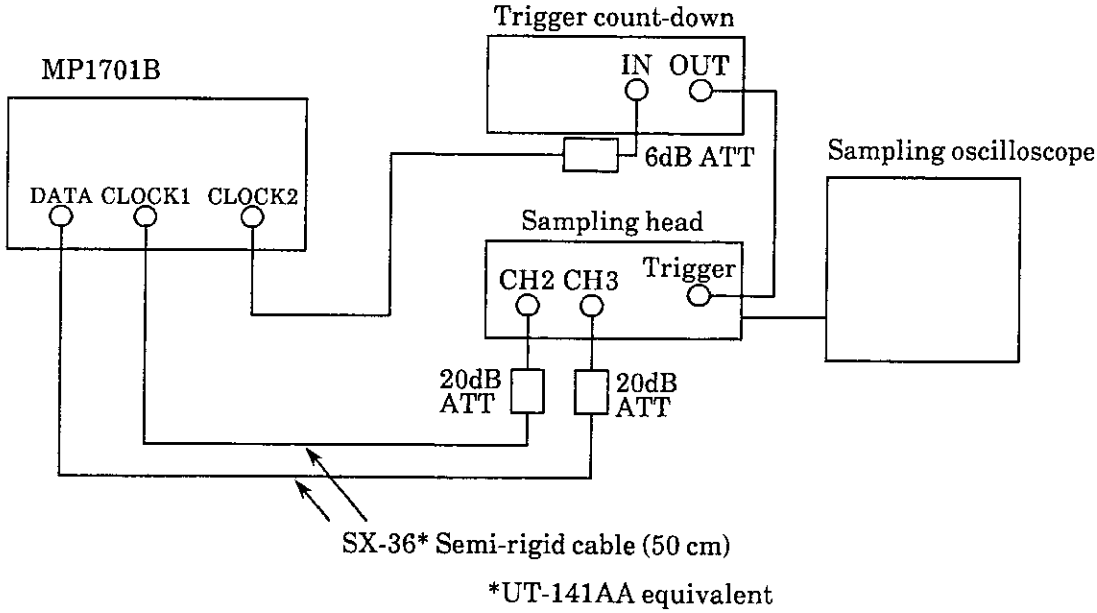


Fig. 7-8 Setup

(3) Procedure

Step	Procedure
1	Adjust both the sampling oscilloscope trigger level and trigger-count-down trigger level to minimize CLOCK1 jitter.
2	Set the MP1701B output pattern to PRBS 2^{15}-1.
3	Measure the DATA jitter in accordance with Fig. 7-7.
4	Change the connection to $\overline{\text{DATA}}$ and measure similarly.

7.3.6 1/4DATA jitter

(1) Specifications

1/4DATA ≦100 ps

(2) Setup

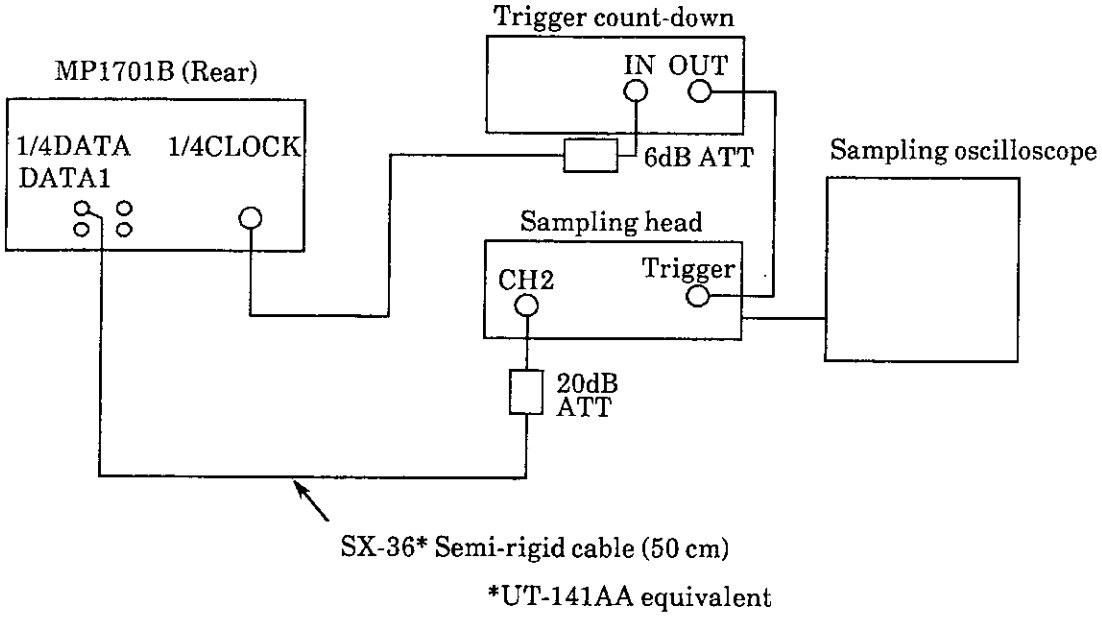


Fig. 7-9 Setup

(3) Procedure

Step	Procedure
1	Adjust both the sampling oscilloscope trigger level and trigger-count-down trigger level to minimize jitter.
2	Set the MP1701B output pattern to PRBS 2^{15}-1.
3	Measure the 1/4DATA1 jitter in accordance with Fig. 7-7.
4	Change the connection to 1/4DATA2 to 4 and measure similarly.

7.3.7 CLOCK1, $\overline{\text{CLOCK1}}$, CLOCK2, 1/4CLOCK rise and fall times

(1) Specifications

CLOCK, $\overline{\text{CLOCK1}}$, CLOCK2 tr, tf

≦30 ps (≧5 GHz)

≦50 ps (<5 GHz)

1/4CLOCK tr, tf ≦200 ps

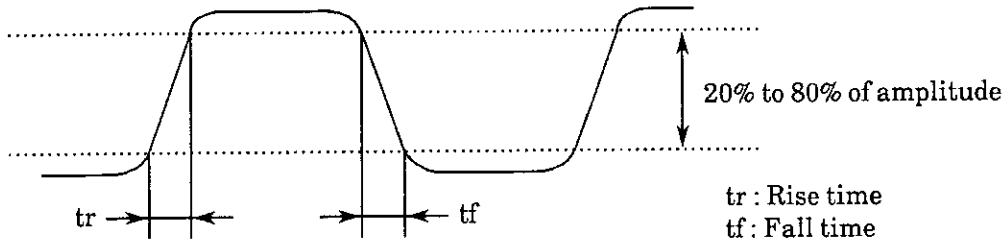


Fig. 7-10 Rise and Fall Times

(2) Setup

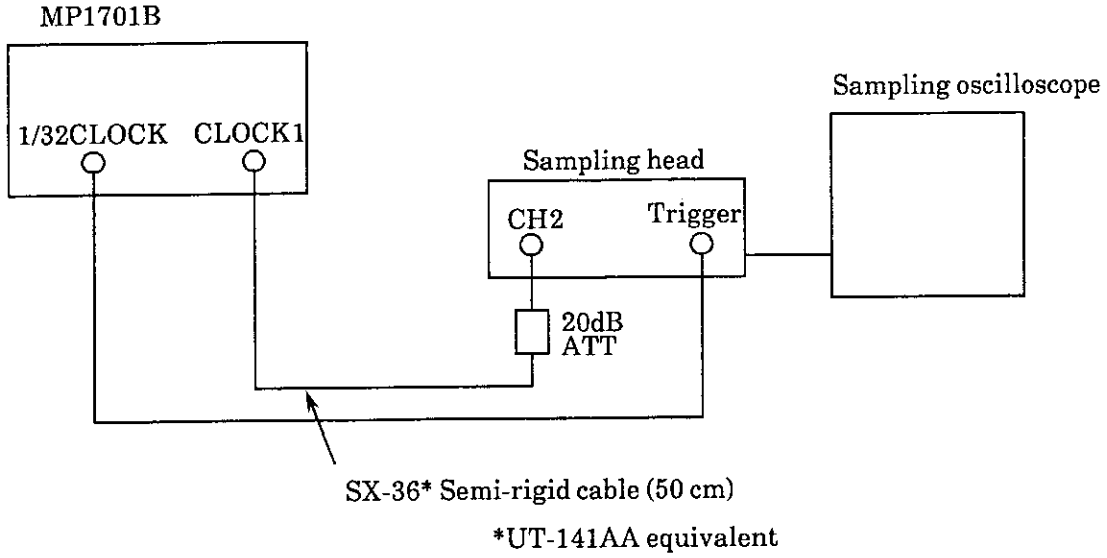


Fig. 7-11 Setup

(3) Procedure

Step	Procedure
1	Adjust the sampling oscilloscope trigger level to synchronize the waveform.
2	Set the sampling oscilloscope mode to average and the bandwidth to 20 GHz (or 34 GHz).
3	Measure the CLOCK1 tr and tf in accordance with Fig. 7-10.
4	Change the connection to $\overline{\text{CLOCK1}}$, CLOCK2, and 1/4CLOCK and measure tr and tf similarly.

7.3.8 CLOCK1, $\overline{\text{CLOCK1}}$, CLOCK2, 1/4CLOCK amplitude and offset voltage

(1) Specifications

CLOCK1, $\overline{\text{CLOCK1}}$ amplitude

0.5 to 2 Vp-p, 10 mV steps

Setting error: ≦ ±15% or ±100 mV, whichever is greater

CLOCK1, $\overline{\text{CLOCK1}}$ offset voltage

−2 to +2 V (V_{OH}), 5 mV steps

Setting error: ≦ ±15%, ±100 mV or ±15% of amplitude, whichever is greatest

CLOCK2 amplitude

2 Vp-p, ≦ ±15%

CLOCK2 offset voltage

0, ≦ ±300 mV

1/4CLOCK amplitude

0.5 to 1 Vp-p, 10 mV steps

Setting error: ≦ ±15% or ±100 mV, whichever is greater

1/4CLOCK offset voltage

−1.5 to +1.5 V (V_{OH}), 5 mV steps

Setting error: ≦ ±150 mV

Fig. 7-12 Amplitude and Offset Voltage

(2) Setup

The setup is the same as that in paragraph 7.3.7 (2) and is shown in Fig. 7-11.

(3) Procedure

Step	Procedure
1	Adjust the sampling oscilloscope trigger level to synchronize the waveform.
2	Set the sampling oscilloscope mode to average and the bandwidth to 20 GHz (or 34 GHz).
3	Measure the CLOCK1 amplitude and offset voltage in accordance with Fig. 7-12.
4	Apply the sampling oscilloscope frequency characteristic correction value to the measured value.

Note: A typical sampling oscilloscope frequency chanracteristic is shown in Fig. 7-13.

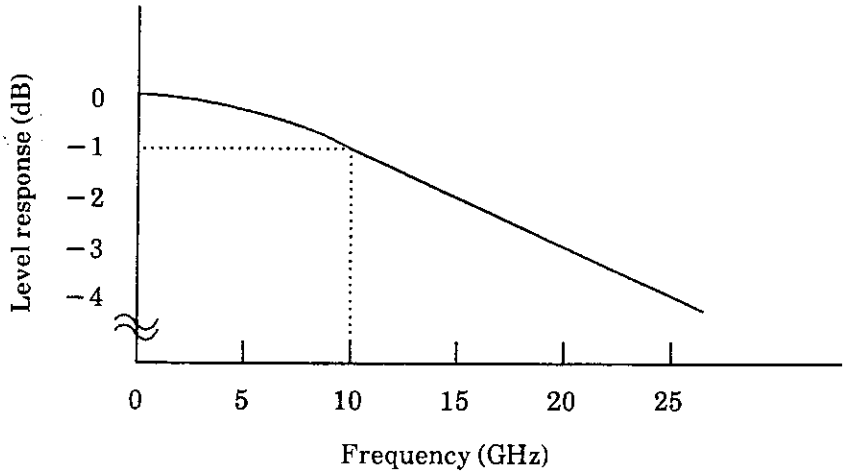


Fig. 7-13 Typical Sampling Oscilloscope Frequency Characteristic

For example, at 10 GHz, since the correction value is −1 dB, the true amplitude is 1.122 times the measured value (1 dB) higher. The true offset voltage is the sum of the measured offset voltage and the measured amplitude multiplied by (1.122−1)/2 = 0.061. This relation is shown in Fig. 7-14.

Step	Procedure

4
(Cont.)

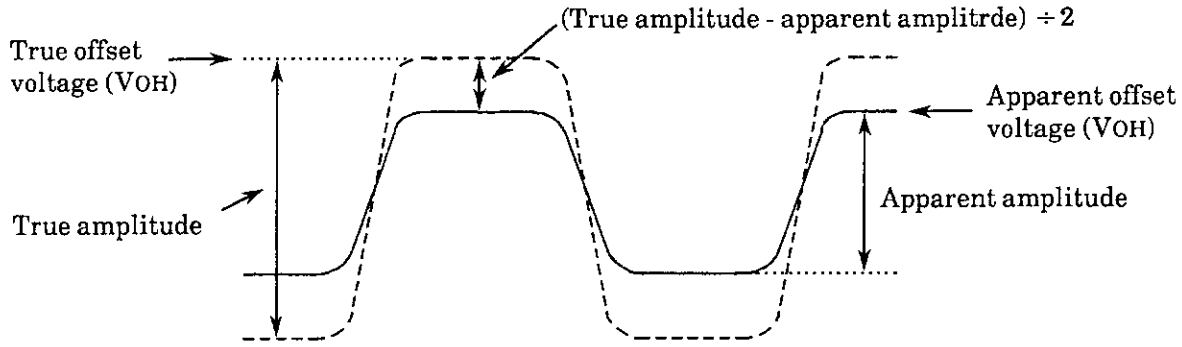


Fig. 7-14 True Amplitude and Offset Voltage

5 Change the connection to $\overline{\text{CLOCK1}}$, CLOCK2, and 1/4CLOCK and measure similarly.

7.3.9 Pattern

(1) Specifications

Pseudorandom pattern

Pattern length: 2^N-1, N = 7, 9, 11, 15, 20, 23, 31

Mark ratio: 0/8, 1/8, 1/4, 1/2 (8/8, 7/8, 3/4, $\overline{1/2}$ also possible by logic inversion)

Programmable pattern

- Data mode

  Data length: 2 to 524 288 bits (128 bit steps for more than 4096 bits)

- Word mode

  Word length: 2 to 16 bits

  Number of words: 1 to 32 768 [When (word length) × (number of words) exceeds 4096, (word length) × (number of words) becomes a multiple of 128.]

(2) Setup

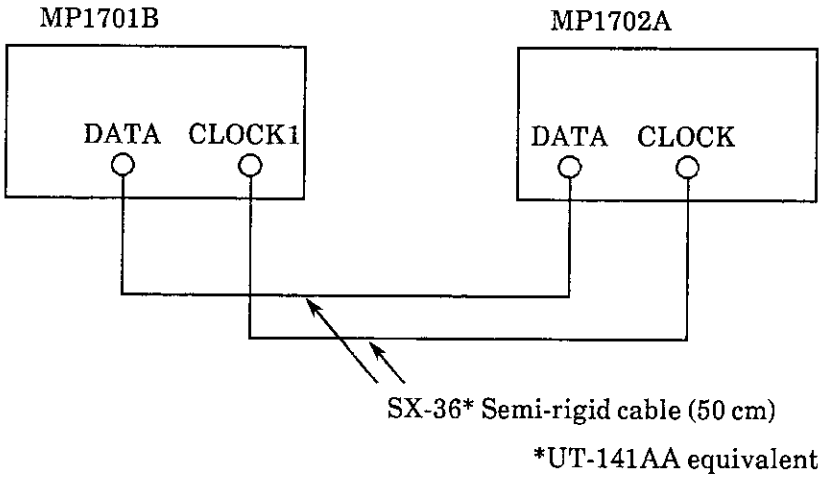


Fig. 7-15 Setup

(3) Procedure

Step	Procedure
1	Initialize the MP1701B.
2	Initialize the MP1702A.
3	Adjust the MP1702A CLOCK PHASE and check if the SYNC LOSS and ERRORS lamps are turned off.
4	Check that the MP1702A ERRORS lamp does not light when MP1701B and MP1702A PRBS PATTERN are changed as follows, 2^7-1, 2^9-1, 2^{11}-1, 2^{20}-1, 2^{23}-1, and 2^{31}-1.
5	Check that the MP1702A ERRORS lamp does not light when MP1701B and MP1702A MARK RATIO are changed as follows, 1/2, 1/4, 1/8, 7/8, 3/4, and $\overline{1/2}$.
6	Set the MP1701B and MP1702A PATTERN to the DATA mode and DATA LENGTH to 524 288 bits. Set the MP1701B BIT appropriately and the MP1702A FRAME SYNC to ON and check if the MP1702A SYNC LOSS and ERRORS lamps go off.
7	Set MP1701B and MP1702A PATTERN to the WORD mode, WORD LENGTH to 16 bits, and NUMBER OF WORDS to 32 768. Set the MP1701B BIT appropriately and chek that the MP1702A SYNC LOSS and ERRORS lamps go off.

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